PLACEMENT OF INTEGRATED CIRCUIT ELEMENTS IN VIEW OF THERMAL MODE

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In this paper we propose criteria and the appropriate approach for the initial placement of integrated circuit cells. The approach provides topological equalization of thermal field, which will increase thermal reliability of IC. The proposed approach makes it possible to simultaneously consider both power equalization and connectivity of elements.

Keywords: topological equalization of thermal field, thermal placement.

According to ITRS the total power consumption of today's ICs is reaching up to 100—150 W, and average density of power consumption is 0.5—0.75 W/mm^2. The prediction says that in the next decade average density of power consumption will rise up to 1.35 W/mm^2. In high-performance ICs the temperature can be higher than 100°C, and the difference of local temperature in semi conductive crystal's different parts can reach 10—20°C [1]. In these conditions the thermal reliability of ICs is very important. During the physical design of ICs one of the effective ways to increase thermal reliability can be decreasing the difference of temperatures in different parts of a semi conductive crystal.

Description of the method

To maintain the highest reliability of IC we must decrease as much as possible the temperature of local high temperature areas. During element placement phase this can be reached using topological equalization of thermal field, which can be represented by the following formula

$$\sum_{i=1}^{n}\left|T_i - \overline{T}\right| \rightarrow \min , \qquad (1)$$

where $\overline{T}$ is the average temperature of IC's elements.

Admitting that thermal exchange in IC's semi conductive crystal is mainly done buy thermal conductivity, which in given thermal mode is described by Fourier's rule, the temperature for some i^{th} element is determined from the condition for mutual thermal influence of elements [2]:

$$T_i = T_0 + \sum_{j=1}^{n} P_j R_{ji} , \qquad (2)$$

where T_0 is environment temperature; P_j is the power of the jth element; R_{ji} is thermal resistance between positions of the ith and j^{th} elements.

If we consider that R_{ij} thermal resistance with first approximation is directly proportional to the d_{ij} distance between the ith and j^{th} elements and that T_0 is constant for all elements, we can represent (1) as subtraction of powers

$$F_1 = \sum_{i=1}^{n}\sum_{\substack{j=1;\\ i\neq j}}^{n}\left|P_i - P_j\right| d_{ij} \rightarrow \min . \qquad (3)$$

From designer's point of view, the result means that elements with greater difference in power should be placed closer. This will reduce the temperature in hot areas by heating up cooler areas.

In traditional element placement algorithms, the minimization of overall length of interconnections is used as main criteria [3]:

$$F_2 = \sum_{i=1}^{n}\sum_{\substack{j=1;\\ i\neq j}}^{n} r_{ij} d_{ij} \to \min, \quad (4)$$

where r_{ij} is the number of connections between the ith and j^{th} elements.

If we compare (3) and (4), it becomes obvious that the closeness of elements implies the increase in both power difference and number of connections. As element placement complex measure, which takes into account the connections between elements as well as IC's thermal regime, following measure is proposed

$$F = a_1 \overline{F}_1 + a_2 \overline{F}_2 \to \min, \quad (5)$$

where $\overline{F}_1$ and $\overline{F}_2$ are normalized values of F_1 and F_2; a_1 and a_2 are weight coefficients.

Depending on design requirements, designer can give a_1 and a_2 values during design process.

The overall quality of placement according to power equalization is measured with the following method

$$K_L = \left(\frac{\max K_{L_i} - \min K_{L_i}}{\max K_{L_i}} \right) 100\%; i = 1,2,...,m, \quad (6)$$

where K_{Li} is specific power of elements in i^{th} area after placement.

Based on the proposed criteria, a few elements of an ISCAS 85 series test circuits were distributed. The simplest placement algorithm was used for a_1 and a_2 coefficient values. Standard digital cell library, developed by "Synopsys Armenia CJSC Educational Department", was used as an elemental base [4]. The comparative results on power topological distribution and the overall length of the interconnections are given in the table below. The half-perimeter model was used to calculate the space between the interconnections [3].

Name of scheme	Number of elements	min K_{Li} / max K_{Li}, nW/(MHz·μm^2)			Total interconnection length, μm		
		a_1=1; a_2=0	a_1=0; a_2=1	a_1, a_2=0,5	a_1=1; a_2=0	a_1=0; a_2=1	a_1, a_2=0,5
C499	202	0,9/2,0	0,7/5,1	0,7/2,7	5226	2594	2991
C3540	1669	2,2/10,2	1,6/18,8	1,8/13,5	52621	28966	31957
C5315	2307	1,8/7,2	1,4/12,0	1,4/8,5	153931	76142	80130

As seen in the table, the power equalization coefficient K_1 has decreased from 4 to 12% compared to the case without the use of power placement, and the total length of inter-connections has decreased from 36 by 45%.

The results show that by increasing ration of a_1 and a_2 coefficients, it is possible to achieve the decrease of power equalization coefficient K_l by 13—31% without significantly increasing the overall interconnection length.

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О. Ж. Арутюнян

Учет теплового режима при размещении элементов интегральных схем

Предложены критерий и соответствующий подход для начального размещения ячеек интегральных схем, обеспечивающие топологическую равномерность распределения теплового поля и, тем самым, повышение тепловой надежности. Предлагаемый подход позволяет совместно с тепловым режимом рассмотреть также электрическую связанность элементов.

Ключевые слова: топологическое выравнивание температурного поля, тепловое размещение элементов ИС.