THERMAL FIELD MODELING OF INTEGRATED CIRCUITS

Tigran Gasparyan

Synopsys Armenia CJSC
Armenia, Yerevan
tigrangs@synopsys.com

The author proposes a simulation method of a thermal field of the semiconductor crystal of integrated circuits, based on the principle of electrothermal analogy. The electric equivalent circuit of heat exchange of IC constructed on current sources and resistance is proposed. The technique of the application is the proposed simulation method at initial multiparameter placement of logic cells of IC. The efficiency of the proposed method is explained on a test example of a logic circuit.

Keywords: integrated circuits, electrothermal modeling, thermal field of crystal, initial placement of cells.

In contemporary IC working temperature of semiconductors can reach more than 100°C and the temperature differences between different areas of the crystal can reach more than 10—20°C [1]. As the reliability of IC mostly depends on its working temperature, it is becoming important to develop such modeling methods of thermal field of crystal which will provide the possibility to estimate efficiently the thermal distribution on surface of the semiconductor crystal during IC designing [2]. This article provides the estimation method of thermal field of crystal based on electrothermal modeling.

Description of the method

The proposed method of electrothermal modeling is based on the construction of electrothermal cell or heated zone of semiconductor crystal. On the basis of electrothermal model of the cell it is possible to create the whole model of IC topology. For c17-ISCAS85 benchmark circuit (see Fig. 1) in case of placing logical cells linearly the electrothermal model will look as presented in Fig. 2.

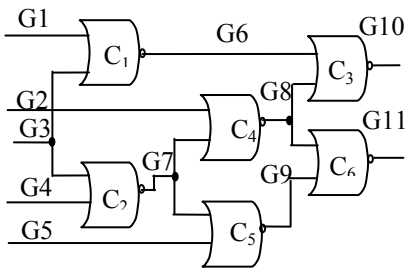

Fig. 1. C17-ISCAS85 benchmark circuit

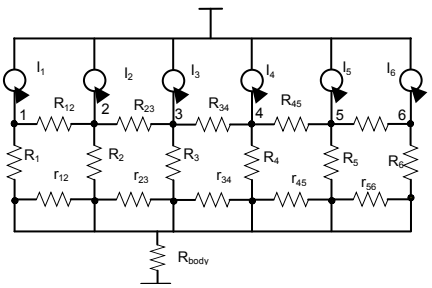

Fig. 2. Electrothermal model of liner placement of c17-ISCAS85 benchmark circuit

In electrothermal model given in Fig. 2 nodes *1—6* represent the placement sequence of the cell. The ambient temperature is not taken into account. It is assumed that the temperature is calculated with respect to the ambient temperature. R_{body} represents the thermal resistance of the IC body. Suggested approach of electrothermal modeling is realized in SPICE modeling system. That is why on the given cells placement we must estimate equivalent circuit parameters taking into account the transfer of thermal parameters into corresponding electrical quantities. Values of R_{ij}, r_{ij} and R_j are estimated with the following equation:

$$R = \frac{d}{\lambda S},$$

where d is a topological distance between centers of cells in case of calculating R_{ij} and r_{ij} or the height of semiconductor substrate in case of calculating R_i; S is surface area of heat exchange; λ — thermal conductivity of the substrate.

Dissipated power unit is estimated by

$P = P_{s.d.p.}KW + P_{st.}$,

where $P_{s.d.p}$ is specific dynamic power of the cell; K is cell switching activity; W is working frequency of the cell; $P_{st.}$ is static power of the cell.

Practical results

Realization of the proposed method is based on the c17-ISCAS85 benchmark circuit (Fig. 1). Parameters of logical circuit are chosen from standard cell libraries of 90 nm which was developed in the educational department of "Synopsys Armenia" [3]. The following values of parameters are taken from mentioned library: topological width — 2.88 μm, topological length of logical cells C_1, C_3, C_5, C_6 — 1.92 μm, C_2, C_4 — 3.2 μm; $P_{1s.d.p.} = P_{3s.d.p.} = P_{5s.d.p.} = P_{6s.d.p} = 15$ nW/MHz; $P_{2s.d.p} = P_{4s.d.p} = 28$ nW/MHz; $W = 300$ MHz. Cell switching active values are taken from testing results: $K_1 = 0.27$; $K_2 = 0.15$; $K_3 = 0.26$; $K_4 = 0.3$; $K_5 = 0.8$; $K_6 = 0.6$. Using the above mentioned values and Form.2 the following power values were calculated: $P_1 = 1.15 \cdot 10^{-6}$ W; $P_2 = 1.26 \cdot 10^{-6}$ W; $P_3 = 1.17 \cdot 10^{-6}$ W; $P_4 = 2.52 \cdot 10^{-6}$ W; $P_5 = 3.6 \cdot 10^{-6}$ W; $P_6 = 2.7 \cdot 10^{-6}$ W. The depths of the active and passive layers of the semiconductor substrate were chosen 3 μm and 10 μm correspondingly. The thermal conductivity of silicon substrate is 1.4 W/(cm·K). Using mentioned values, the following values of resistors were calculated: $R_{ij} = 5 \cdot 10^{-4}$ Ohm, $r_{ij} = 0.5 \cdot 10^4$ Ohm, $R_i = 2 \cdot 10^4$ Ohm. Thermal resistance of substrate is: $R_{body} = 1.2 \cdot 10^7$ Ohm. Using SPICE modeling the following voltage values were received in the following cases:

a) logical cells connectivity only: U_1=43; U_2=44; U_3=45; U_4=45.5; U_5=46;
b) power distribution uniformity: U_1=43,5; U_2=43,5; U_3=43; U_4=44; U_5=43,5;
c) both a) and b) : U_1=43; U_2=43,5; U_3=44,5; U_4=45; U_5=44;

Digital values of temperature of heated areas (in °C) will be equal to corresponding voltage with adding environment temperature value. Testing results show that the initial placement of the logical cells power will bring to higher (70—80%) uniformity of thermal field.

Conclusion

The electrothermal modeling method allows representing the placement of the thermal field of IC as identical electrical scheme where thermal parameters are replaced by corresponding electrical ones. The built electrical scheme can be analyzed by SPICE. Such solution allows creating electrothermal models for various topological structures.

REFERENCES

1. Semiconductor Industry Association, International Technology Roadmap for Semiconductors, 2003, http: // public.itrs.net/

2. Арутюнян А. Г. Повышение равномерности распределения теплового поля при начальном размещении топологических ячеек ИС // Труды III Всероссийской науч.-техн. конфер. «Проблемы разработки перспективных микро- и наноэлектронных систем».— Москва: ИППМ РАН, 2008.— С. 251—254.

3. Digital Standard Cell Library//SAED_EDK90_CORE DATABOOK: © 2008 SYNOPSYS ARMENIA Educational Department.— Yerevan, 2008.

———————

Т. Гаспарян

Моделирование теплового поля интегральных схем

Предложен метод моделирования теплового поля кристалла полупроводниковых интегральных схем (ИС), основанный на принципе электротепловой аналогии, и соответствующая электрическая схема замещения теплообмена ИС. Приведена методика применения предложенного метода моделирования при начальном многопараметрическом размещении логических ячеек ИС. Эффективность данного метода разъяснена на тестовом примере логической схемы.

Ключевые слова: интегральная схема, электротепловое моделирование, тепловое поле кристалла, начальное размещение ячеек.