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COMPARISON OF GATE DELAY MEASUREMENTS IMPLEMENTED VIA HSPICE AND PRIMETIME TOOLS

K. Sloyan, Dr.Sc. V. Melikyan

Synopsys Armenia CJSC
Armenia, Yerevan
sloyan@synopsys.com

The purpose of this paper is to compare the gate delay dependence on supply voltage and output capacitance as the results of static and dynamic timing analysis. The study has been conducted via PrimeTime and HSPICE tools which implement the said timing analysis respectively.

Keywords: gate delay, power voltage, capacitance, static timing analysis, dynamic timing analysis.

The current trend of technologies leads to scaling down of process technologies. It affects the following major characteristics of integrated circuits: speed performance, power consumption, PVT (process, voltage, temperature) variations, etc., which are essential factors in circuit design nowadays. Those aspects have their influence on gate delay in circuits. It is known that power dissipation is approximately proportional to the square of the supply voltage in digital CMOS circuits [1]. Decrease of supply voltage will lead to reduction of power consumption at the expense of increased gate delay. Speed performance increases year by year [2] with the scaling down of technologies [3] and it is inversely proportional to the gate delay. Variations in the process parameters can be impurity concentration densities, oxide thicknesses and diffusion depths. This introduces variations in the sheet resistance and transistor parameters such as threshold voltage. The threshold voltage decreases with the channel length of MOS transistors [4] which consequently brings gate delay changes [5]. Temperature is one of the most important parameters in circuit design which impacts on gate delay too. The propagation delay increases with increased temperature [6].

The impact on the gate delay via above mentioned parameters for various technologies has been observed in the past. For instance, in [1] a study has been conducted that observes the dependency of the threshold and supply voltage on gate delay time for 0.5 μm technology. In the work, lowering supply voltage reduces power consumption, but some issues arise, such as the gate delay increase which is illustrated in the second part of the paper [1].

This work presents gate delay dependence on supply voltage and output capacitance of a gate in case of 90 nm technology. In the first part, it is observed the comparison of dependency between supply voltage and gate delay implemented via HSPICE [7] and PrimeTime tools [8]. The second section of the paper represents comparison of dependency between output capacitance and gate delay implemented by the same tools.

Simulation method

Timing analysis can be static and dynamic. Dynamic timing analysis (DTA) verifies functionality of the design by applying input vectors and checking for correct output vectors, whereas static timing analysis (STA) checks static delay requirements of the circuit without any input or output vectors. Quality of DTA increases with the increase of input test vectors. But increased test vectors increase simulation time. STA does not require input vectors and has a runtime that is linear with the size of the circuit [8]. DTA can be implemented by HSPICE and VCS whereas STA by PrimeTime (PT) tools.

In this paper the dependencies among gate delay, supply voltage and capacitance of the gate for the standard cells have been obtained for 90 nm technology. All experiments have been done for NAND standard cell. Input data files and parameters to get above mentioned dependencies by HSPICE are illustrated in Tab. 1 and 2.

Table 1

Input data for HSPICE simulations

Input data	
netlist(.spi)	description of transistors and power sources
SAED90nm.lib	models and electrical parameters ofMOS transistors, diodes, resistors
deck (.sp)	are included the netlist and .lib technology file

Table 2

Input parameters of HSPICE deck

Input parameters	
operating frequency	300MHz
rise time of input data	50ps
fall time of input data	50ps
supply voltage	1.2V
output capacitance	4fF

PrimeTime tool controls gate work through the switch of clock signal. But since NAND cell does not have such internal signal there is need to introduce virtual clock which plays the same role as a real clock signal. Some constraints which are put on input and clock signal are the followings:

```
create_clock -name vclk -period 2 -waveform {2 3}
set_clock_transition -fall 0.03 [get_clocksvclk]
set_clock_transition -rise 0.03 [get_clocksvclk]
set_input_transition -rise 0.05 {in1}
set_input_transition -fall 0.05 {in1}
```

PrimeTime needs some technology libraries which are obtained based on above mentioned .lib file in-the result of cell characterization. It takes information about all pins of cells and calculates gate delay time through input transition time and output capacitance [8].

Experiments and results

The main aim of this paper is to compare the results obtained by HSPICE and PrimeTime tools. At first we observe dependency between supply voltage (VDD) and propagation gate delay (t_{pd}). Below are mentioned the results of highlighted tools (see Tab. 3).

Comparing those two results we notice that the results obtained via HSPICE is more accurately than those implemented via PrimeTime tool (Fig. 1).

The next observation is the dependency between output capacitance load (C) of the gate and its propagation delay (t_{pd}) obtained by the mentioned tools(see Tab. 4).

It is known that the dependence between propagation delay of a gate and output capacitance is linear [1] which proves the results of simulations as well (Fig. 2).

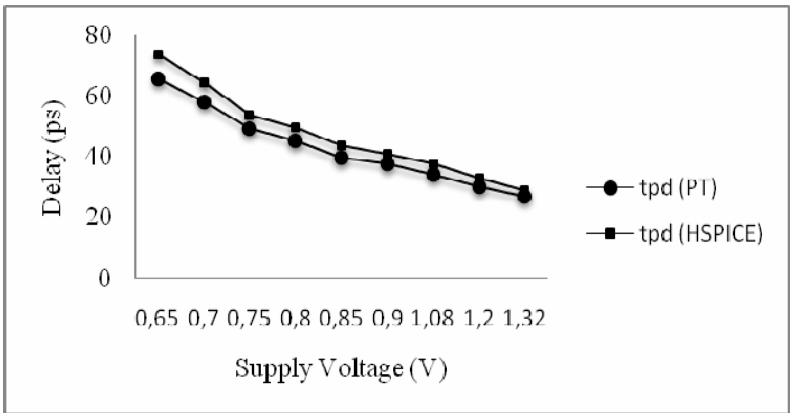

Fig.1. Propagation delay dependence on supply voltage via HSPICE and PT tools

Table 3

Gate delay values for different supply voltages

	t_{pd} (ps)	
VDD (V)	HSPICE	PT
0.65	73.5	65.5
0.7	64.5	58
0.75	53.5	49
0.8	49.5	45
0.85	43.5	39.5
0.9	41	37.5
1.08	37.5	34
1.2	33	30
1.32	29	27

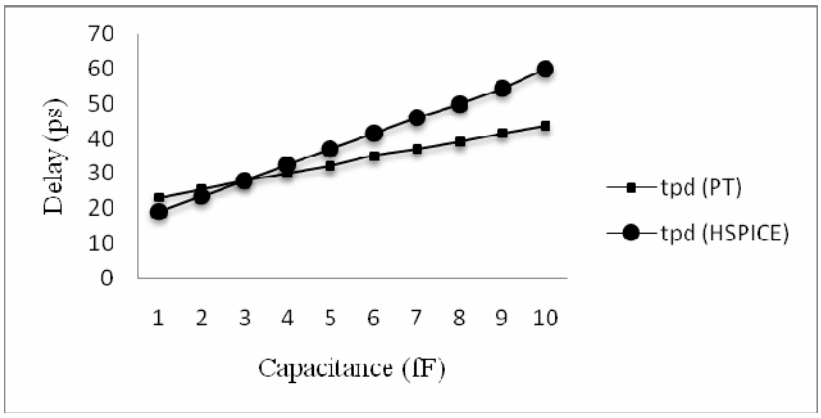

Fig. 2.Gate propagation delay dependence on output capacitance via HSPICE and PT tool

Table 4
Gate delay values for different output capacitances

	t_{pd} (ps)	
C (fF)	HSPICE	PT
1	19	23
2	23.5	25.5
3	28	28
4	32.5	30
5	37	32
6	41.5	35
7	46	37
8	50	39
9	54.5	41.5
10	60	43.5

Conclusion

In this paper, study of gate delay dependence on supply voltage and output capacitance is conducted. This study is led by HSPICE and PrimeTime tools which are widely used in industry for gate delay measurement capabilities. The results show that HSPICE model is more accurate compared to PrimeTime model. Also, both models reveal linear dependency between output capacitance load and propagation delay which is consistent with other studies.

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К. Слоян, В. Меликян

Сравнение результатов измерений задержки затвора, осуществленная с помощью инструментов HSPICE и PrimeTime.

Целью данной работы является сравнение зависимости задержки затвора от напряжения питания и выходной емкости как результатов статического и динамического анализа времени. Исследование было проведено с помощью инструментов HSPICE и PrimeTime, которые реализуют, соответственно, упомянутый анализ времени.

Ключевые слова: *задержка затвора, напряжение питания, емкость, статический временной анализ, динамический временной анализ.*