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TECHNOLOGY OPTIONS FOR EMBEDDING LOW-PROFILE ELECTRONIC COMPONENTS IN PRINTED CIRCUIT BOARDS

In order to improve the overall characteristics of printed circuit boards, two technologies for the formation of multilayer printed circuit boards have been developed – with the embedding of low-profile electronic components in a layer of fiberglass and a monolithic layer of polyimide, provided that they are assembled without soldering and welding. The indicators for quantitative evaluation of printed circuit boards with embedded electronic components and their comparison both among themselves and with printed circuit boards without embedded electronic components are proposed.

Keywords: embedded electronic components, printed circuit boards, low-profile electronic components, connecting layers, polyimide varnish.

Size and weight reducing of modern electronic devices, while increasing their functionality, performance and reliability is possible through the use of new electronic technologies and to a large extent is provided by the improvement of electronic components (**EC**), first of all, of integrated circuits and their packaging technologies. The increase in the number of leads and a decrease in their pitch, more frequent use of matrix arrangement of leads under the package, the integration of several devices on the chip and several components in one package, impose specific requirements for printed circuit boards (**PCB**). To increase the density of joints, besides the use of such means as reducing the size of the elements of the printed pattern and increasing the number of layers, interlayer and contact connections, it is necessary to find other solutions that allow better adaptation of the development of electronic components to the design of electrical connections on PCB.

Such solutions should make the design process more flexible and improve the PCB characteristics, primarily electrical and electromagnetic compatibility.

One of these perspective design and technological solutions is PCB with embedded ECs, for which it is possible to use the term «hybrid integrated circuit board» [1–5].

For the last 5–6 years, this direction of the development of printed circuits in electronic equipment has been fully formed and continues to be improved, besides it is regarded as one of the directions that determine the development of radio electronics [1].

Embedded electronic components are components inserted inside a usually multilayer PCB. They can be of two types: formed – these are ECs that are created during the manufacturing of PCBs on its internal layers (can only be passive) and inserted – these are independently produced discrete components that are placed on the inner layer of a PCB during its manufacturing or assembly (may be both passive and active, have small dimensions, first of all thickness). More information about the design and technological solutions for creating PCBs with embedded ECs can be given in **Fig. 1** classification of PCBs [6].

Due to the fact that today the PCBs with inserted electronic components have great potential and, thus, greater interest in use, we consider the technological processes of embedding discrete components.

There are a number of design and technological solutions for the creation of printed circuit boards with embedded ECs. All of them have their own peculiarities, advantages and disadvantages, areas of application. Most of them contain SMD components for embedding that are installed on the inner layers of fiberglass and fixed by adhesive. In order to form electrical connections, operations typical for surface mounting are used. The fiberglass layers with embedded components are then pressed together with connecting layers of semiproduct material prepreg. Thus, the ECs are placed in the connecting layers.

Such a constructive and technological approach to the implementation of PCBs has some disadvantages, primarily due to the fact that the elec-

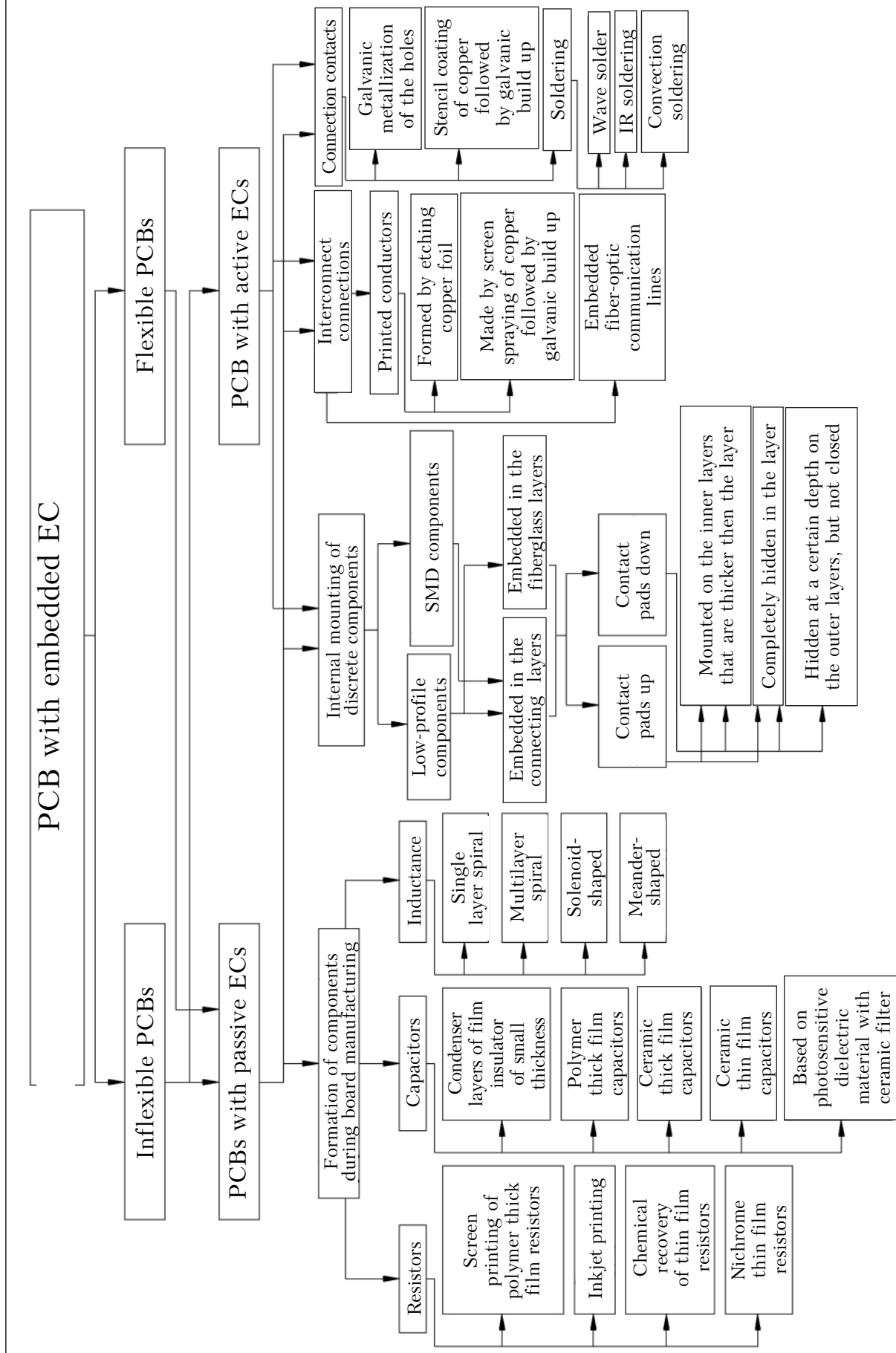


Fig. 1. Classification of PCBs with embedded ECs [6]

tronic components used are relatively thick, and also the need to carefully select the technological parameters of the pressing process in order to avoid damage to the installed ECs during its conducting [9]. It is possible to reduce the thickness of a multilayer PCB by using low-profile (LP) ECs [10]. However, there are certain problems associated with the fact that since the contact pads of such ECs are made by spraying and have copper surfaces [10], they can not be mounted by soldering. The inability to use conventional soldering operations of SMD components determines the need to create new technologies for mounting LPECs.

The purpose of this study was to develop of technology for the creation of printed circuit boards with improved overall dimensions with embedded electronic components and their installation without soldering and welding.

Within the framework of the solution of the problem, the authors developed two versions of the PCB manufacturing technology: embedding low-profile ECs into the fiberglass layer and embedding low-profile ECs into the monolithic polyimide layer. Furthermore, coefficients are proposed that allow evaluating the efficiency of using embedded ECs.

The technology of embedding ECs into a fiberglass layer

The difference between this method and the known ones [5–9] is that the components occupy a volume directly in a layer of fiberglass, and not in the connecting layer.

Besides, instead of the usual SMD components, special LPECs are used which have the same electric parameters but lower height (Fig. 2).

The technology of the formation of multilayer printed circuit boards with embedded LPECs is considered on the example of implementation of

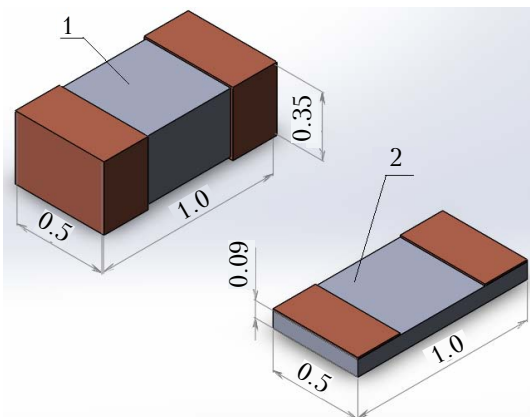


Fig. 2. Overall dimensions of SMD (1) and low-profile resistor (2) of type 0402

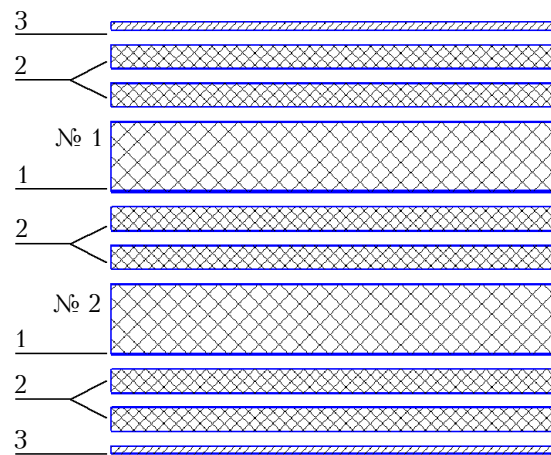


Fig. 3. The initial structure of a multilayer PCB: 1 – cores №1 and №2 (foil-coated fiberglass); 2 – connecting layers (prepreg); 3 – copper foil

a 6-layer printed circuit board (Fig. 3) with such parameters [11]:

- cores (inner layers) 1 made of a double-sided fiberglass with a thickness of 300 μm with a 5 μm thick foil on both sides (material FR4 0.3/5/5);
- connecting layers 2 of a type 2116 prepreg film with a thickness of 105 μm . Allowable number of connecting layers in the multilayer printed circuit boards is at least 2 and not more than 4;
- outer layers of copper foil with a thickness of 35 μm (may vary).

It should be noted, that the possibility of using a single bonding layer depends on the nature of conductor pattern of the printed circuit board and the thickness of adjacent copper layers. The thicker is the copper layer and the greater is the density of the conductor pattern, the more difficult it is to fill the space between the conductors with resin, and the quality of the filling affects the reliability of the board. This is why, for example, for a 35 μm thick copper foil layer, one can use only a type 7628 connecting layer with a thickness of 180 μm .

Total thickness of the assembled board, taking into account shrinkage of the connecting layers, is about 1.3 mm.

In this example, we embed two type 0402 LP resistors and a type 0402 LP ceramic capacitor on core №1, a type 1206 LP ceramic capacitor on core №2, and a type 0402 SMD resistor on each of the outer layers. The ratio of the dimensions of these components is shown in Fig. 4.

The first technological operation in the PCB manufacturing process is the preparation of cores for the ECs installation, which involves the creation of through holes for installing components

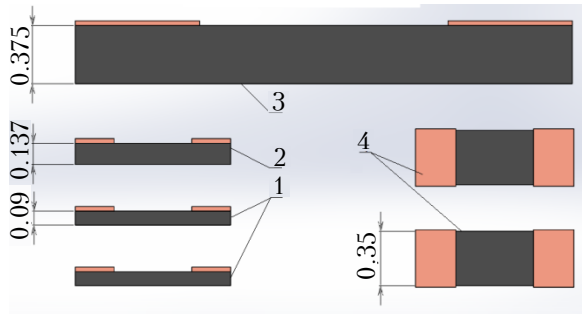


Fig. 4. The ratio of the dimensions of ECs:
1 – type 0402 LP resistors; 2 – type 0402 LP ceramic capacitor; 3 – type 1206 LP ceramic capacitor; 4 – type 0402 SMD resistors

in them and through holes for further formation of interlayer electrical connections. The holes for the ECs installation can be of two types: round and rectangular. Round holes can be made by means of mechanical drilling and laser cutting. Rectangular holes can be cut with a laser. It should be noted, that to maintain the integrity of the structure of fiberglass, it is of course best to use laser cutting along the contour. According to this technology, for type 0402 components (resistors and capacitors) we cut out round holes, and a rectangular hole is made for the type 1206 capacitor (Fig. 5). The cross section of a multilayer PCB with holes for the EC is shown in Fig. 6.

The next technological operation is placing and fixing the ECs in their corresponding holes (Fig. 7). To fix the EC, it is necessary to put the correspond-

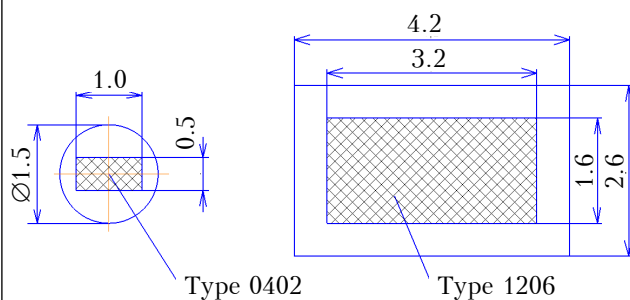


Fig. 5. ECs in their installation holes

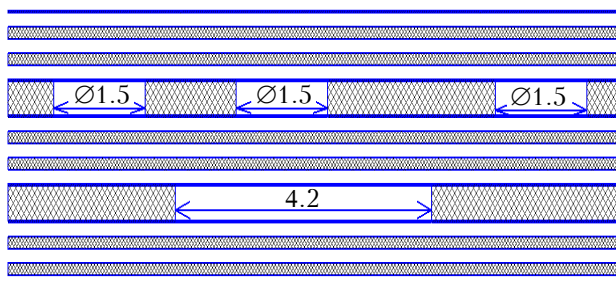


Fig. 6. Cross section of a multilayer PCB with holes for electronic components in internal layers

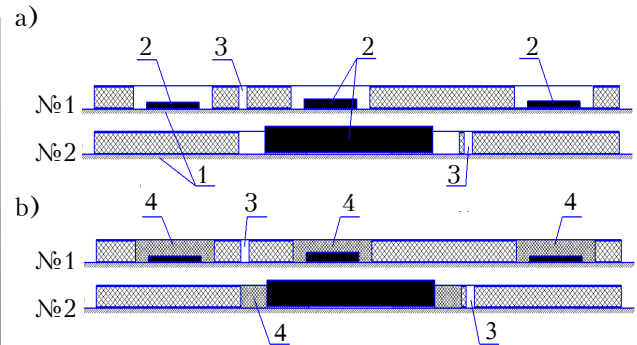


Fig. 7. Mounting (a) and fixing (b) of LPECs on cores №1 and №2:

1 – flat surface; 2 – ECs; 3 – through transition hole; 4 – polyimide varnish

ing core on a smooth flat surface, then to insert the component into the corresponding hole in such a way that the contact pads are oriented downwards and touch the supporting surface. Contact pads must be precisely oriented according to positions, determined by the layout of the ECs on the PCB. After that, it is necessary to fill the void with the ECs in such a way that the polyimide varnish fills the entire thickness of the inner layer. For filling holes with installed ECs, it is offered to use polyimide varnish or epoxy resin.

After polymerization of the varnish, it is necessary to electrically connect the EC contact pads with the core copper foil layer. This is realized by means of screen printing deposition of a copper layer up to 3 μm thick on the corresponding sites (Fig. 8). At the same time, copper is sprayed into the through holes for the interlayer connections. Note, that in cases of high density of the conductor pattern on the inner layers, it is possible to perform a screen deposition of copper on the sites that were formed during the polymerization of the varnish.

Then a number of normal operations are performed:

- photoresist application;
- projecting the PCB pattern through the photo mask, which should be positive, that is, the conductor pattern should be opaque, so that after the photoresist is developed, it remains on the blank spaces of the board;
- developing the photoresist, washing off unexposed areas and washing the PCB;
- galvanic buildup of an at least 25 μm thick copper layer on a conductor pattern, including the transition holes;
- deposition of metal resist layer (tin-lead alloy);
- photoresist removal;
- etching of copper in blank spaces and washing the board.

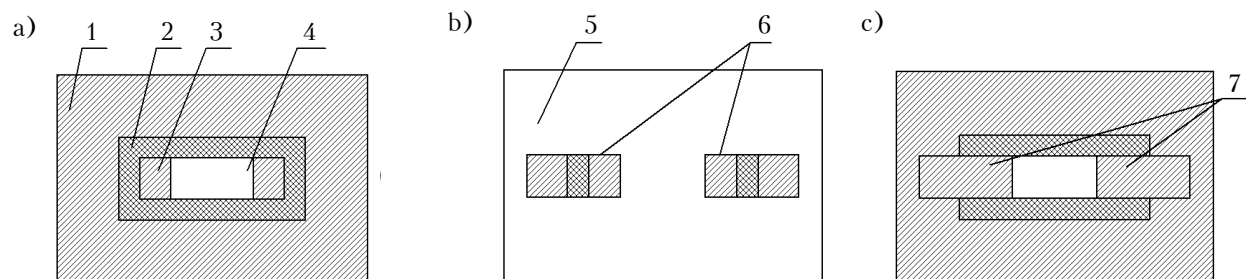


Fig. 8. Stages of screen copper sputtering to create contact connections:

a – preparation of PCB for sputtering; *b* – PCB with a screen; *c* – PCB with the formed contact connections;
 1 – copper foil ; 2 – polyimide film; 3 – LPEC contact pads; 4 – LPEC; 5 – screen; 6 – screen holes integrating the contact pads of EC with a layer of copper foil; 7 – sputtered copper layer

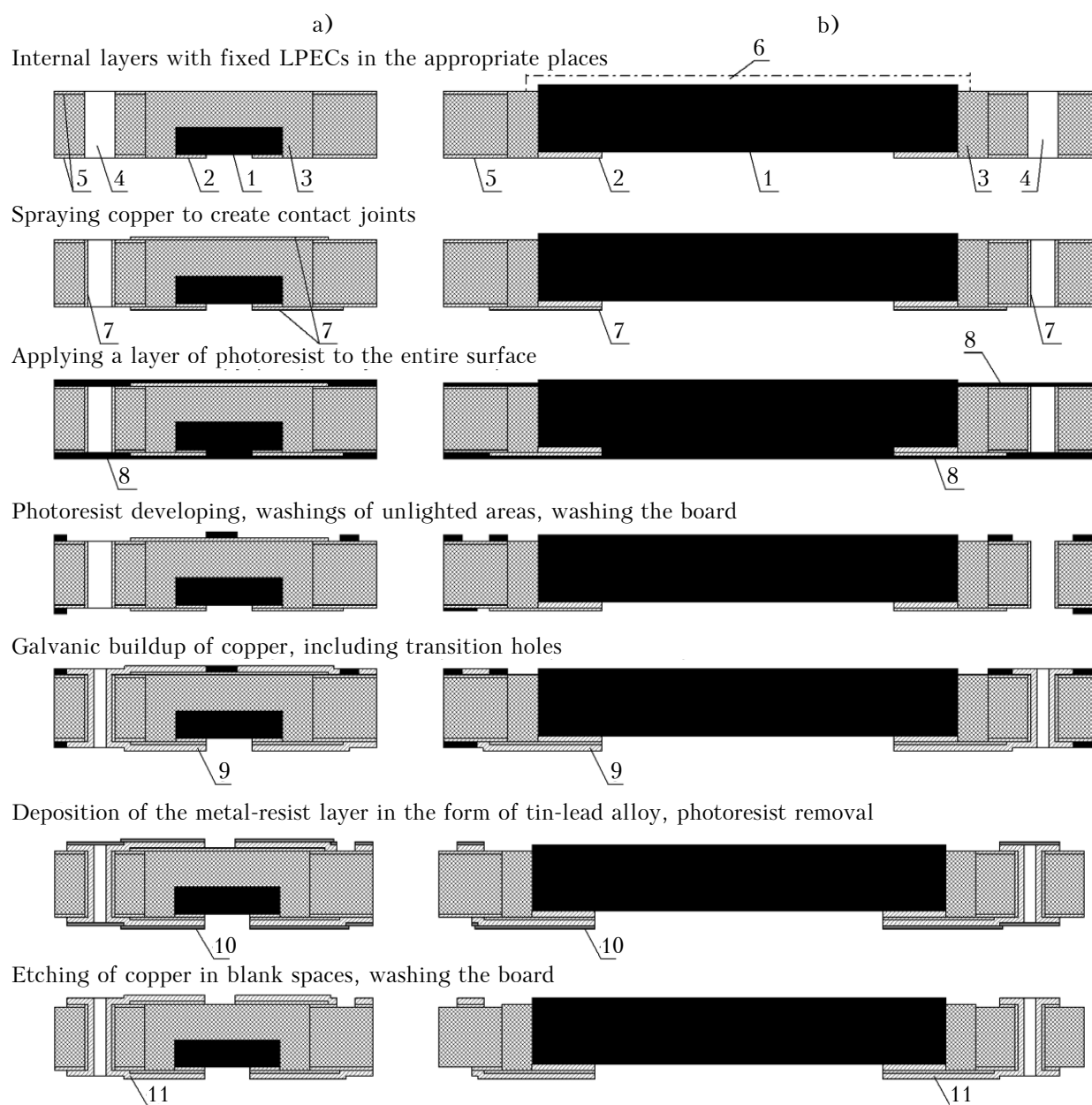


Fig. 9. Scheme of the process of conductor pattern formation on cores №1 (*a*) and №2 (*b*):

1 – LPEC; 2 – contact pads LP EC; 3 – polyimide film; 4 – through holes; 5 – copper foil; 6 – restricted area; 7 – deposited copper layer; 8 – photoresist layer; 9 – electroplated copper layer; 10 – metal resistor layer; 11 – conductor pattern

The conductive pattern is formed on both sides of the core as two layers interconnected by means of metallized holes.

It is more difficult to create a conductor pattern on the side of the PCB opposite the contact pads of the ECs. When the components protrude beyond the level of the filled varnish, a forbidden zone is formed in which it is impossible to create a conductor pattern. In cases, when the EC packages are sensitive to the corrosive environment formed during the manufacturing process, they need to be isolated.

Fig. 9 presents a diagram of the above described technological process of combining contact pads of low-profile ECs with core copper layers and creating such a conductor pattern where one EC is fixed in each inner layer: a type 0402 capacitor in core №1; type 1206 capacitor in core №2.

The prepared internal PCBs (cores) are pressed to each other and to the outer foil layers with interconnecting layers between them (Fig. 3). When pressed, the layers are heated in order to facilitate the filling of all internal cavities with the connecting layer. Pressing regimes do not differ from those used in the process of pressing multilayer PCBs manufactured, for example, by through-hole metallization. As a result of pressing, printed circuit boards shown in **Fig. 10** are obtained.

It should be noted that the embedded low-profile ECs are limited in thickness — in case some part of the EC protrudes over the core, its

height should be less than the thickness of the connecting layer, taking into account its shrinkage during pressing. This limitation is due to the limited thickness of the connecting layers. The thickest connecting layer is the type 7628 prepreg of “Shengyi” [10, 11], its thickness is 0,185 mm before pressing and 0,180 mm after pressing. Also, the more commonly used cores have thickness of 0,300–0,450 mm, so the embedded components can have a thickness of not more than 0,810 mm, but to reduce the mechanical load during pressing, it is not advisable to use ECs with a thickness close to the boundary values.

In our example, the thickness of the largest selected EC is 0,375 mm, the thickness of the core with a two-sided conductor pattern is about 0,350 mm and the thickness of the connecting layers after pressing is 0,100 mm. Thus, after the pressing of a multilayer PCB, the minimum thickness of the connecting layer between the inner layers should be about 0,150 mm, which satisfies the indicated restriction.

The next technological operations are the drilling of through holes and their subsequent metallization (**Fig. 11**).

To create a finished multi-layer PCB, it is necessary to form a conductor pattern on the outer layers of copper foil, which is done using standard operations.

Installation of the SMD and possibly other ECs is also performed using standard technologies. A fragment of the electronic module with

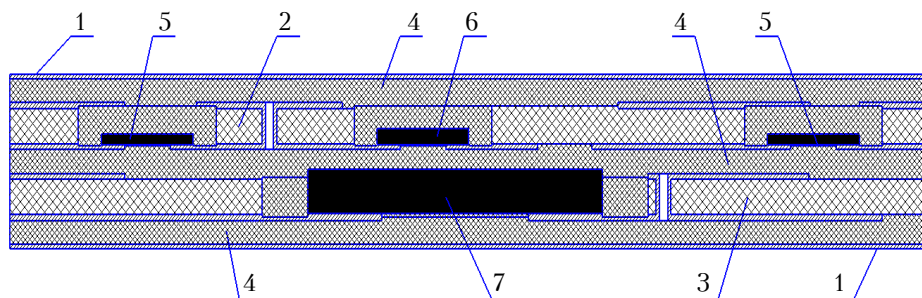


Fig. 10. The result of pressing all layers of the multilayer PCB:

1 — outer copper foil; 2 — inner layer №1 with type 0402 embedded resistors (pos. 5) and a type 0402 capacitor (pos. 6); 3 — inner layer №2 with a type 1206 embedded capacitor (pos. 7); 4 — connecting layers

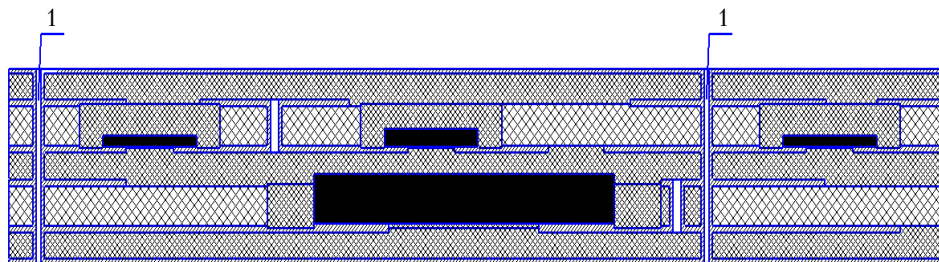


Fig. 11. The formation of through holes 1 with their subsequent metallization

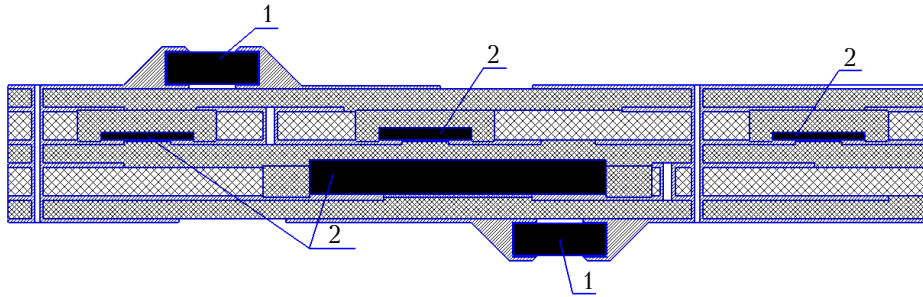


Fig. 12. Electronic module on a multilayer PCB with surface mounted components (1) and with embedded low-profile ECs (2)

external ECs for surface mounting on a multilayer PCB and with embedded ECs is shown in **Fig. 12**.

Thus, the thickness of the considered multilayer PCB with embedded ECs is about 1.5 mm, that corresponds to the thickness of the PCB, more often used in electronic equipment design practice. The described technological process allows embedding components of larger dimensions than those considered in the example.

Thus we can conclude that this technology of embedding elements can compete with the already known technologies, in which the components are embedded into the connecting layer, and not into the inner layers of fiberglass.

The technology of embedding ECs in a monolithic polyimide layer

As a result of the embedding ECs into the PCB according to this technology, an inner layer with embedded ECs is a monolithic structure that is formed by filling the form with installed LPECs by polyimide varnish, followed by its polymerization and the formation of a conductor pattern on this film. The sequence of operations for implementing such a solution is shown in **Fig. 13**.

Here we give some explanations to technology operations given in Fig. 10.

- The low-profile ECs are installed in a special form, the size of which is determined by the size of the PCB that is created. Contact pads of the components should be oriented downward and fixed in the proper places.

- Polyimide varnish can be poured into the mold to a level when some components will be completely filled and some will protrude, or to such level when all components are completely varnished. In the first case, on the side of the board opposite the EC pads, a forbidden zone is formed, where it is impossible to create a conductor pattern.

- The 3 μm thick copper layer is formed using screen deposition, and electrical connections of the EC contact pads with a copper layer are formed. At the same time, copper is sprayed into transition holes to form the interlayer connections.

Galvanic buildup of a conductor pattern is carried out until a copper layer with a thickness of at least 25 μm is obtained.

With such monolithic polyamide layers with embedded components and conductor pattern, it is possible to form a multilayer PCB. Such boards are based on polyimide and are thus characterized by a certain flexibility. For those cases where some rigidity of the board is required, one or more layers of glass fiber laminate can be added to the structure of the multilayer PCB.

Indicators for quantitative evaluation of PCB

To give quantitative evaluation of the design and technological solutions of a PCB and assemblies with embedded ECs the authors propose several indicators that can be used for comparison of the PCBs with embedded ECs to each other, and to the PCBs without the embedded ECs.

- Coefficient of use of embedded ECs

$$K_{USE} = N_{EEC} / N,$$

where N_{EEC} is the number of embedded ECs;

N is the total number of ECs on a PCB.

- Coefficient of use of embedded components for the area

$$K_{USES} = \sum_{i=1}^{N_{EEC}} S_{EECi} / \sum_{i=1}^N S_i,$$

where S_{EECi} is the installation area of the i^{th} embedded component;

S_{EECi} is the installation area of any i^{th} EC.

The coefficient of use (K_{USES}) can be used for more accurate estimation of the degree of use of the embedded EC in comparison with the coefficient K_{USE} .

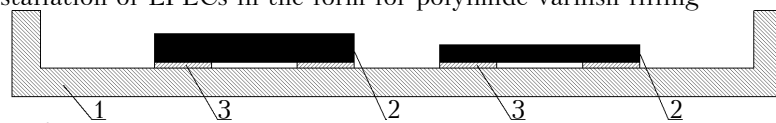
- The efficiency factor of the embedded EC use for the area of the PCB:

$$K_{EFS} = S_{PCB} / S_{PCB EEC},$$

where S_{PCB} is the area of the PCB without the embedded ECs;

$S_{PCB EEC}$ is the area the same PCB with the embedded ECs.

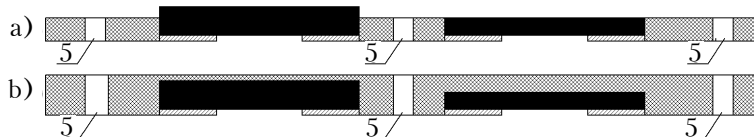
Installation of LPECs in the form for polyimide varnish filling



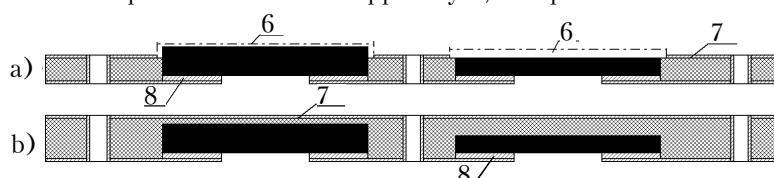
Form fill with polyimide varnish



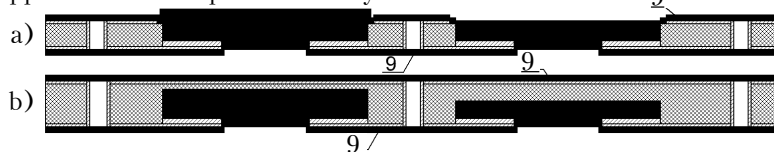
Drilling through transition holes



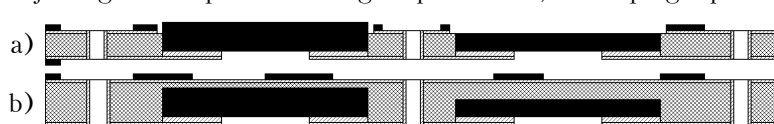
Screened deposition of a solid copper layer, except for forbidden zones



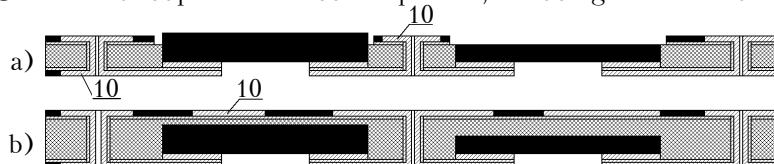
Application of the photoresist layer on the whole surface



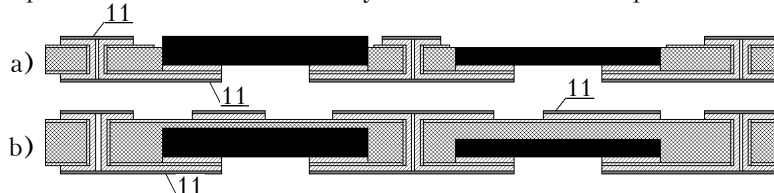
Projecting a PCB pattern through a photomask, developing a photoresist, washing the board



Galvanic buildup of the conductor pattern, including in the transition hole



Deposition of the metal resist layer and removal of the photoresist



Eching copper from blank spaces, washing the board

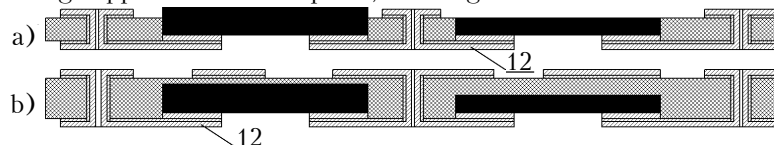


Fig. 13. The technology of creating monolithic polyimide layer with embedded low-profile ECs not completely varnished (a) and completely varnished (b):

1 – form for filling; 2 – low-profile ECs; 3 – ECs contact pads; 4 – polyimide; 5 – through holes; 6 – restricted area; 7 – copper deposited layer; 8 – contact pads connected with a copper layer; 9 – photoresist; 10 – galvanically built up copper layer; 11 – metal resist; 12 – conductor pattern

– The efficiency factor of the embedded ECs use for the height of the PCB:

$$K_{Efh} = h_{PCB} / h_{PCB\ EES},$$

where h_{PCB} is the height of the PCB without embedded ECs;

$h_{PCB\ ECC}$ is the height of the PCB with embedded ECs.

– Length reducing factor for the connections on the printed circuit board:

$$K_L = L / L_{EES},$$

where L_{PCB} is the total length of the connections on the PCB without embedded ECs;

L_{EEC} is the total length of the connections on the PCB with embedded ECs.

It should be noted that the problems that arise in high-speed electronic modules are associated with signal integrity [12, pp. 260–263], which, in turn, depends on the length of electrical connections. So, using the K_L factor you can indirectly evaluate the printed circuit boards by the integrity of the signals being transmitted.

Conclusions

Thus, two versions of the EC embedding technology in printed circuit boards have been developed: embedding low-profile ECs in the fiberglass layer and in a monolithic layer of polyimide in the conditions of their installation without soldering or welding. Both methods allow improving the overall characteristics of printed circuit boards with embedded electronic components and can compete with known technologies. The indicators proposed for the quantitative evaluation of various design and technological solutions can help in carrying out studies of PCBs with embedded electronic components for their further development.

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ВАРІАНТИ ТЕХНОЛОГІЇ ВБУДОВУВАННЯ НИЗЬКОПРОФІЛЬНИХ ЕЛЕКТРОННИХ КОМПОНЕНТІВ У ДРУКОВАНІ ПЛАТИ

Друковані плати (ДП) з вбудованими електронними компонентами є більш складними конструкціями у порівнянні зі звичайними багатошаровими ДП, але, без сумніву, мають переваги і перспективи при вирішенні проблем мікромініатюризації електронних пристроїв. Технології для їх реалізації постійно розвиваються, а також, що особливо важливо, збільшується номенклатура електронних компонентів (ЕК), адаптованих для вбудовування.

Вбудовані електронні компоненти — це компоненти, розташовані всередині, як правило, багатошарової структури ДП. Вони можуть бути двох типів: сформовані — це ЕК, які створюються у процесі виготовлення ДП на її внутрішніх шарах (можуть бути тільки пасивними); вставлені — це незалежно виготовлені дискретні компоненти, які розміщують на внутрішньому шарі ДП в процесі її виготовлення чи збірки (можуть бути як пасивними, так і активними, мають невеликі розміри, в першу чергу товщину).

У даній роботі з метою покращення габаритних характеристик друкованих плат розроблено технології утворення багатошарових ДП з вбудованими низькопрофільними (НП) електронними компонентами у шар склотекстоліту та у монолітний шар полііміду, які монтуються без паяння та зварювання. Перший спосіб вбудовування відрізняється від відомих тим, що компоненти розміщуються не у сполучному шарі, а займають об'єм безпосередньо у шарі склотекстоліту. При використанні другої технології внутрішній шар із вбудованими ЕК є однією монолітною конструкцією, яка утворюється за допомогою заливання форми з встановленими НП ЕК поліімідним лаком з подальшою його полімеризацією та виконанням провідникового рисунку на цій плівці. Обидва способи дозволяють покращити габаритні характеристики друкованих плат з вбудованими електронними компонентами і можуть конкурувати із відомими технологіями.

Крім того, для кількісного оцінювання різних конструкторсько-технологічних рішень ДП в роботі запропоновано показники, які можуть допомогти при проведенні досліджень ДП із вбудованими ЕК для подальшого їх розвитку.

Ключові слова: вбудовані електронні компоненти, друковані плати, низькопрофільні електронні компоненти, сполучні шари, поліімідний лак.

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ВАРИАНТЫ ТЕХНОЛОГИИ ВСТРАИВАНИЯ НИЗКОПРОФИЛЬНОЙ ЭЛЕКТРОНИКИ В ПЕЧАТНЫЕ ПЛАТЫ

Печатные платы (ПП) со встроенными электронными компонентами являются более сложными конструкциями по сравнению с обычными многослойными ПП, но, без сомнения, имеют преимущества и перспективы при решении проблем микроминиатюризации электронных устройств. Технологии для их реализации постоянно развиваются, а также, что особенно важно, увеличивается номенклатура электронных компонентов (ЭК), адаптированных для встраивания.

Встроенные электронные компоненты — это компоненты, расположенные внутри, как правило, многослойной структуры ПП. Они могут быть двух типов: сформированные — это ЭК, которые создаются в процессе изготовления ПП на ее внутренних слоях (могут быть только пассивными); вставленные — это независимо изготовленные дискретные компоненты, которые размещают на внутреннем слое ПП в процессе ее изготовления или сборки (могут быть как пассивными, так и активными, имеют небольшие размеры, в первую очередь толщину).

В данной работе с целью улучшения габаритных характеристик печатных плат разработаны технологии образования многослойных ПП со встроенными низькопрофільними (НП) електронними компонентами в слой склотекстоліта і в монолітний шар полііміда, які монтируються без пайки і зварки. Перший спосіб встраивания отличается от известных тем, что компоненты размещаются не в связующем слое, а занимают объем непосредственно в слое склотекстоліта. При использовании второй технологии внутренний слой со встроенными ЭК является одной монолитной конструкцией, которая образуется с помощью заливки формы с установленными НП ЭК полиимидной лаком с последующей его полимеризацией и выполнением проводникового рисунка на этой пленке. Оба способа позволяют улучшить габаритные характеристики печатных плат со встроенными электронными компонентами и могут конкурировать с известными технологиями.

Кроме того, для количественной оценки различных конструкторско-технологических решений ПП в работе предложены показатели, которые могут помочь при проведении исследований ПП со встроенными ЭК для дальнейшего их развития.

Ключевые слова: встроенные электронные компоненты, печатные платы, низькопрофільні електронні компоненти, соединительные слои, полиимидной лак.