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METHODS AND MECHANISMS OF GETTERING SILICON STRUCTURES IN FABRICATION OF THE INTEGRATED CIRCUITS

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Element base integration rate increase presents ever more strict requirements to concentration reduction of the polluting impurities and oxidation defects of packing in the initial silicon wafers with its preservation in the process cycle of the IC fabrication. This governs the high application actuality of gettering in the modern technology of microelectronics. There were considered the existing methods of gettering the silicon wafers, as well as the methods of their progress.

Key words: silicon, getter, laser, fast diffusing impurity, center of gettering, dislocation, defect of packing.

Arrangement density increase of the integrated microcircuit (IC) elements ensues the stricter requirements to purity of the semiconductor materials, as presence of the crystal structure defects and metal impurities in it affects their functionality. Foremost, this concerns silicon, which is the basic material for IC fabrication. A great contribution to this is made by the point defects and polluting impurities, such as copper, iron, nickel, chrome, sodium, etc., resulting in the yield reduction of the good ICs due to the uncontrolled process of the defect formation in the active areas. The requirements to purity of the silicon wafers in bulk and by surface are being steadily made ever stricter parallel to reduction of the critical size of elements, reaching the detection limit when determining the surface concentration of metals and iron bulk concentration (see **Table 1**) [1]. Density parameter of the packing oxidation defects (POD) also serves the surface purity criterion, and the requirements to its value are quite strict. Reduction of the element sizes requires application of the new materials and technological processes of their fabrication, which results in expansion of the metals nomenclature and reduction of the critical value of their surface concentration. Thus, with the size of elements being 0,8 μm the critical concentration value for each of metals, forming silicides (Cr, Fe, Ni, Cu)**,** constitutes $1 \cdot 10^{11}$ atom / cm^2. With transition to the sizes of less than 0,8 μm, this row is extended with Co, alkali metals K, Na, whose ions are mobile, as well as the alkaline earth element Ca and heavy metals Pt, Ir, Ba. The critical value of concentration for each of these elements constitutes $\leq 1 \cdot 10^{10}$ atom/cm^2 [1].

Table 1

Requirements to Purity of the Silicon Wafers of Various Diameter for the Purpose of Fabrication of the Dynamic Operational Memory Device

Feature	Diameter of Wafer, mm					
	150	200	200	200	300	300
Minimum size of element, um	0,8	0,35	0,18	0,13		0,09
Iron bulk concentration, atom / cm^3	$5 \cdot 10^{10}$	$2 \cdot 10^{10}$	$\leq 1 \cdot 10^{10}$	$\leq 1 \cdot 10^{10}$		$\leq 1 \cdot 10^{10}$
Metals surface concentration, atom / cm^2	$1 \cdot 10^{11}$	$2 \cdot 10^{10}$	$\leq 1 \cdot 10^{10}$	$\leq 1 \cdot 10^{10}$		$\leq 1 \cdot 10^{10}$
POD density, cm^{-2}	$\leq 6 \cdot 10^{1}$	$\leq 2 \cdot 10^{1}$	$\leq 4{,}4 \cdot 10^{0}$	$\leq 2{,}8 \cdot 10^{0}$		$\leq 1{,}6 \cdot 10^{0}$

The main sources of the polluting impurities are the accessories and equipment, used in the different technological processes of ICs fabrication [2]. In principle, material pollution starts already in the growth process of the silicon mono-crystals by the Chokhralsky method. The sources of impurities here are the initial poly-crystal silicon, quartz crucible and the furnace itself [3]. However, meanwhile the grown ingots are considered pure enough, as the impurities concentration is not high: Fe, Cu and other metals are of the numerical values of less than 10^{14} cm^{-3} [4].

The major polluting operations during fabrication of substrates are the mechanical slicing and polishing. This is pointed out by distribution of the metal impurities in the wafers — their grater part is localized in the near surface layer with the thickness of the order of a few micrometers from the surface [2].

Pollution with the uncontrollable impurities occurs also during the multiple heat treatments in the diffusion furnaces, to which a silicon wafer is subjected in the process of IC creation [2]. At the high temperature the quartz reactors let the metal atoms «pass», evaporating from the internal surface of the surface metal parts (usually Fe, Ni, Cr, Cu), which afterwards diffuse into the wafer bulk [4]. In the plants for the epitaxial growth of wafers the potential source of impurities is a graphite heater, that in the heating process emits the transitional metals, for instance Fe, Ti.

Pollution probability of the silicon wafers with the metal impurities is also evident during cleansing, rinsing, transportation of wafers [5], ion implantation [6] and plasma chemical treatment [7]. As a result, concentration of the metal impurities in the silicon wafer bulk during the heat treatment process may reach 10^{18} cm^{-3}, and in the near surface area it is one – two orders higher [2, 7]. As during the temperature reduction solubility on many metals reduces in silicon, their concentration during the wafer cooling supersedes the solubility limit, and this causes their diffusion to the wafer surface, precipitation and complex formation of metals with the doping impurities [8]. Formation of metal precipitates affects the parameters of both bipolar and MOS-devices. Small metal precipitates (from 5 to 20 nm) are the sources of the current leakage in the bipolar transistors [9] and the source of the localized breakdown in the thin oxide films [10]. As the centers of the heterogeneous nucleation, required for precipitation, there may serve defects of the crystal structure, such as dislocations, defects of packing (predominantly on the partial dislocations) and oxygen precipitates. Packing defects, decorated with

the metal impurities, also cause the leakage currents rise and breakdown of the thin oxide [10].

Influence of the transitional metals, such as Fe, Ni, Cu, Cr on yield of good ICs and their reliability at the technology level of 0,5 um becomes noticeable with the concentration of, for instance, Fe ions of the order 10^{11} cm^{-3}. Also, it is assumed, that when the capacity of the random access memory devices becomes close to Gb with the thickness of the gate oxide of 7,5 nm, the limit of the permissible iron concentration will fall to the level of 10^{10} cm^{-3} [4].

It is possible to substantially reduce the amount of the uncontrollable impurities in the silicon wafers, introduced in the process of the entire cycle of ICs fabrication by means of applying the appropriate measures. For instance, this may be the temperature reduction in the process of the periodical high temperature cleansing of the quartz pipes in the medium of HCl, utilization of the advanced furnace designs, for instance, double pipes, displays [11]. Chemical treatment of wafers prior to thermal treatment in the mixtures of H_2O_2 and HCl, HF and ethanol makes it possible to reduce the amount of metal pollutions on their surface [12]. Besides, replacement of components of the ion implantation plants, plasma chemical etching, made of the stainless steel, for aluminum, silicon and carbon made substantially reduces the overall pollution level [2].

However, all this does not make it possible to avoid pollution of the silicon wafers with the uncontrollable impurities and generation in them of the point defects in the process of fabrication of the semiconductor devices. In view of this, at present of great significance for this purpose acquire the process methods — methods of gettering [2, 13]. They make it possible to create in the silicon wafer the pure from the structural defects and the polluting mechanical impurities near surface area, in which are formed the active and passive elements of the IC areas. According to [1], gettering is the process of dissolving the unadvisable impurities with their subsequent diffusion and precipitation in the specially created zones of wafers — getters, where they do not exert the detrimental influence on operation of the device. A getter is capable of grasping and keeping the fast diffusing impurities and point defects, as well as creates the conditions, ensuring their high mobility [14].

During fabrication of the contemporary microelectronic devices the problem of purity becomes one of the most global ones, meanwhile what is meant is purity at all stages of the overall cycle of their fabrication. Therefore quite actual is the search of recommendations for the correct selection of the method of gettering in the various cases. For this in the present article are classified the existing methods of gettering with the analysis conducted of the methods of their passing.

There exist the various methods of gettering, differing with location of a getter relative to the operational side of the wafer, the gettering phase and the method of its creation [15].

Getter may be located outside the wafer, on the non-working side of the wafer, on the working side between the elements, in the bulk of the wafer. As a rule, the preference is attributed to the first two methods.

In order to obtain the solid gettering phase the following methods are used:

- mechanical introduction of irregularities
  - — by abrasive treatment;
  - — by sand blasting treatment;
  - — by impact treatment;
- formation of film on the wafer's surface
  - — of porous silicon;
  - — admixture-silicon glass;
  - — poly-silicon;
  - — thermal and pyrolytic film of SiO_2;
- irradiation of the surface
  - — ion doping;
  - — laser irradiation;
  - — ion implantation of inept gases;
- diffusion doping;
- annealing as per the preset program.

Gettering by the gaseous phase is used during the wafer annealing in the various media:

- annealing in vacuum;
- annealing in the inept medium;
- annealing in the chlorine containing medium.

Gettering by means of the liquid phase is used during application of

- the amorphous liquid phase;
- fustible eutectic.

Amongst the methods with location of the getter outside the wafer of wide application are the methods, based on extraction of the point defects to the gaseous phase and to vacuum. In [16] it is established, that annealing of the silicon wafers and ingots prior to oxidation influences generation of the packing defects. Performance of the preliminary annealing of the wafers at the temperature of 800—1200^{o} C in the argon atmosphere reduces density of the packing defects in them, meanwhile the size of defects does not depend on the time of annealing. This is determined by resorption in process of such treatment of the growth defects and migration of their constituting atoms to the surface, being a drain for them. Thus, the pre-oxidation high temperature annealing makes it possible to create the layer in the near surface area, practically free from the packing defects. Thickness of this layer depends on the annealing time (t), and incubation time ($t_и$) — on the initial length of the surface packing defects and the annealing time. With $t > t_и$ thickness of the area, vacant from the given defects (d), varies as per the law $d \sim t^n$, where $n = 0{,}63 \pm 0{,}06$.

The efficient method of gettering is introduction of the mechanical irregularities into the reverse side of the wafer, which are done mostly by grinding [17], sand blasting treatment [18], diamond polishing [19]. N this case gettering is determined by damages of the crystal lattice, which are capable of eradicating the defect buds and adsorbing impurities at the time of the high temperature treatment. For instance, grinding of the reverse side of the substrate prior to oxidation reduces density of the packing defects by three orders. However, on the other side, creation of the disturbed layer results in

emergence of dislocations in the epitaxially grown layers and their gettering of the fast diffusing impurities. Besides, the gettering layer causes the curve of the semiconductor wafers, and the rough reverse side grasps the impurities during the chemical treatment and thus pollutes the wafer. It is also noteworthy noticing, that the mechanical treatment is usually performed prior to the fabrication process of the semiconductor devices, consequently, at the time of the high temperature treatments there occurs a partial re-crystallization of the disrupted layer, resulting in release of its grasped impurity [20].

In order to preclude the given phenomena in [21, p. 8] the following method of gettering was offered. In the reverse side of the wafer by means of grinding the disruptions of the crystal lattice are introduced for the depth of 8—25 um. Then the wafers are subjected to annealing in the inept medium at the temperature and duration of the process, sufficient for gettering the fast diffusing impurities and release of the mechanical stresses. After the thermal treatment the prompt cooling is performed, and further the both sides of the wafer are polished up to the unruffled surface. As a result, on the side of the wafer, in which the irregularities were introduced, under the unruffled surface the disrupted layer remains, gettering the point defects during the subsequent technological processes.

Amongst the contemporary methods of gettering with use of the mechanically disrupted layer is the hydro-abrasive gettering [1]. This method is attractive, as it is easily embedded into the technology of the chemical-mechanical polishing of the silicon wafers, because a getter is created on the reverse side of the of the ground-etched wafer, and formation of the gettering centers and the process of gettering proper occur simultaneously with the first thermal oxidation. The basic variable parameters of the process are the pressure of the hydro-abrasive stream at the nozzle exit, which may vary within the limits of 200—500 kPa, as well as the distance from the nozzle to the wafer surface. Other parameters of the process – the angular velocity of displacement of the table with the wafers, the frequency of the nozzle oscillations, composition of the applied abrasive are constant. The given method is quite effective — it makes it possible to reduce density of the micro-defects (small etching pits) by two orders and by two-three orders – defectiveness of the gate dielectric.

One more method — pre-oxidation gettering [16, 22] is in creation of the stressed layer by means of applying aluminum oxide or silicon nitride with the subsequent annealing , promoting diffusion to it of the point defects. Efficiency of gettering depends on thickness of the stressed layer, time and temperature of annealing and increases, if prior to the film oxidation to the reverse side of the wafer by means of the phosphorus diffusion to introduce the non-conformance dislocation. In order to attain the maximum efficiency, thickness of the applied layer of silicon nitride should constitute 200—400 nm, and annealing of the wafer to be conducted in the inept medium within 1—4 hours at the temperature of 1000—1200 ^{o}C. The non-conformance dislocations are created by means of phosphorus diffusion at 1050—1150 ^{o}C during 1—7 hours. The stressed layer and the non-conformance dislocations, formed in the initial wafer, getter both the available in it point defects and the introduced ones

during the subsequent treatments. It is noteworthy marking, that for the gettering of of the impurity defects by means of the phosphorus diffusion, its concentration should not obligatorily ensure formation of the non-conformance dislocations, as the diffusive layer without dislocations also possesses the gettering action [23], however, smaller, than with the dislocations.

Gettering of the fast diffusing admixtures may be conducted by means of the thin layer of the porous silicon, formed on the reverse side of the wafer by the anode treatment in the etching acid [24]. The given films possess the effect of gettering owing to their high specific surface and the high mechanical stresses on the boundary with silicon [25]. Of such properties are the films of the poly-crystal silicon [26] and germanium [27].

Popular is the method of gettering with application of the phosphorus doped diffusion layer [28], which is created on the reverse side of the wafer prior to the oxidation process. It was established, that the effect of gettering in this case exist and without the non-conformance dislocations and depends on the phosphorus concentration [29]. Efficiency of the process becomes considerable, if the phosphorus concentration exceeds 10^{20} cm^{-3}. With the phosphorus concentration of 10^{21} cm^{-3}, concentration of gold in the wafer bulk reduces to 1000 times because of formation of the ion pairs between gold and phosphorus [30]. It is to be noted, gettering is possible by the boron doped diffusion layers, however, efficiency in this is smaller, than in the case of the phosphorus doping [26].

Of the gettering properties are also the silicon layers, disrupted by the ion doping [31]. Efficiency of such layers is determined by the type of the implanted ion and reduces in the row of O, P, Si, As, B [32]. The type of disruptions is determined by the kind of ions, dose, energy, existence or absence of the oxide protective film, temperature of the wafer during the ion implantation, orientation of the wafer and the annealing mode [33]. At the time of annealing the disrupted layer there are formed the dislocation loops, the packing defects, which act as the centers of gettering. Thus, disruptions of the crystal lattice, created by the ion doping, are used for gettering the polluting impurities from the targets of silicon imaging devices. For the satisfactory operation of the target the leakage current of one diode should not exceed $5 \cdot 10^{-14}$ A at the voltage of 30 V (diodes with the increased leakage currents produce the dark spots on the video image). The main cause, resulting in occurrence of the leakage currents, was formation of the non-coherent precipitates of the polluting impurities. For gettering into the reverse side of the wafer were introduced the ions of phosphorus, arsenic, argon with the energy of 50 keV and the various doses with the subsequent annealing in the dry nitrogen with addition of O_2 during 30 min. The comparative analysis of the gettering effect showed, that the video-defects vanish with the phosphorus doping doses — 10^{16} cm^{-2}, arsenic — 10^{15} cm^{-2} and argon — $3 \cdot 10^{15}$ cm^{-2}. The important peculiarity of such kind of gettering is, that it passes at a high speed at the relatively low temperatures. Thus, a film of gold with the thickness of 0,15 um, applied on the reverse side of the wafer, during 16 hours of annealing at the temperature of 500 ^{o}C completely dissolves, diffuses through the wafer with the thickness of 250 um and crystallizes in the kind of individual grains on the argon implanted (10^{16} cm^{-2}, 250 keV) side of the wafer.

Ion doping is also applied for creation of the internal gettering layer, located somewhat deeper the future device area (about 0,8 um for the designed at the present time ICs). In such a case the drains for the fast diffusing admixtures are the structural silicon defects, created in the substrate's bulk [34]. On efficiency of the internal gettering the following factors exert influence [35]:

- density of the small defects in the substrate's bulk, playing the role of drains for the detrimental impurities;
- availability of the near surface layer, free from the crystal defects, worsening quality of the electronic devices;
- preservation of the gettering centers in the wafer's bulk during the entire process of IC creation.

One of the most acceptable methods of creation of such a gettering layer, possessing the high efficiency (as the drain area for the admixture atoms), is implantation into the working surface of the silicon wafer of hydrogen or helium at the room temperature with the subsequent annealing at the temperature of 800—900 ^{o}C during from several dozens of minutes to one hour [36]. Such a procedure results in formation of the layer containing the gas bubbles at the depth, in conformance with the project run. This is determined by the low solubility of the implanted atoms in silicon, what promotes their segregation into the small gas vacation complexes already at the implantation stage. The subsequent annealing results to growth of such complexes and formation of bubbles. The implanted into silicon hydrogen or helium may during annealing leave the area of bubbles, penetrate the surface layer of silicon and evaporate from the surface already at the temperature, far below the melting point [37]. And this means, that in dependence on the gas concentration and the conditions of annealing, it is possible to obtain the layer, containing interstice, actually not containing the gaseous phase. The similar defects are very efficient drains (traps) for the unadvisable impurities. The ruptured chemical ties on the internal walls of interstice grasp the impurity atoms, which results in emergence of gradient in distribution of their concentration near the layer, containing the interstice. This gradient plays the role of the moving force, stimulating diffusion of impurities from the devices area to the great area, to the area of interstice. For the several types of impurities their concentration may be lower by several orders [37].

Other approach to creation of the internal getter, well compatible with the technology of IC fabrication, is creation of the oxygen precipitates with silicon in bulk of the silicon wafer, being efficient drains for the alien impurities, and creation of the defectless near surface zone (pure zone) for formation of the active IC structures. Pure zone and the layer of the bulk defects — these two most important factors, governing efficiency of the internal gettering, which was demonstrated way back in 1970—80 years [38, 39]. The generally recognized formation pattern of such a getter is the definite heat treatment conductance sequence of the silicon wafers [40]. The first heat treatment, high temperature (1100—1200°C) one, is intended for formation in the near surface area of the zone wafer, depleted by oxygen (because of its evaporation). The second heat treatment, low temperature (600—800°C) one, is

intended for origination of the oxygen precipitation centers. At the third stage, high temperature (>900°C) one, on the oxygen precipitation centers, disintegration occurs of the oxygen solid solution and growth of the oxide precipitates, serving drains for the unadvisable impurities from the working areas of the wafer.

At the last time the method of developed of creation of the oxygen precipitates in silicon, the so called magic depleted area, based on the accelerated oxygen precipitation in the areas, enriched with vacancies (the definite vacation profile is created by means of the fast thermal annealing [1]. Differences of the formation mechanism of the depleted with micro-defects near surface area in this case from the traditional method is in the following. In the traditional method of the internal gettering concentration of vacancies in the wafer's bulk is small and constant by the wafer's thickness, while concentration of the internode oxygen is great in the wafer's bulk and diminishes to the surface. In the formation method of the magic depleted zone the situation is different: concentration of the internode oxygen is permanent by the wafer's cross-section, and concentration of the «hardened» vacancies is great and constant in the wafer's bulk and diminishes to the surface. In the traditional method of the internal gettering there may be used only those silicon ingots (or its parts),in which concentration of the internode oxygen is within the limits $(7,5—9,0)\cdot10^{17}$ atom/cm^3, when the precipitation process is steady and the bulk density of precipitates reaches 10^{11} cm^{-3}. While resorting to the second method of the oxygen concentration, the thermal prehistory of obtaining the ingot and the location of the sliced from it wafer is of no significance. Besides, efficiency of the second method practically does not depend on the thermal cycle of obtaining the device structures. When creating the internal getter by this method there forms the deeper with a sharper boundary, the depleted near surface area (50—60 μm), suitable, opposite to the traditional method, for creation of the structures with the slit isolation.

An interesting method of gettering was offered in [41]. Unlike the methods, when the undesirable impurities although are removed from the working areas of the semiconductor wafer, but nonetheless are available in their vicinities, here the method is used, applied for the zone cleaning of the silicon ingots from the admixture matters in the solid state: under influence of the temperature gradient the impurity is removed to the ingot's butt surface and then etched off. An indirect confirmation of suitability of this idea for gettering the impurity in the semiconductor wafers is movement of the oxygen atoms under influence of the temperature gradient during formation of the buried layers of SiO_2 by means of the non-isothermal annealing of the ion-doped with oxygen of the silicon areas. Simulation of such process showed, that irrespective of the initial distribution of the impurity in the near surface area, under influence of the temperature gradient it concentrates on the wafer surface and can be removed with the subsequent etching of the surface layer off.

The original approach for purification of the silicon wafers' bulk from the undesirable impurities is described in [42]. It is based on application of the ultrasonic treatment of the wafers at the room temperature at the frequency of 0,4—1 MHz and duration up to 6,5 hours. As the strongest influence

ultrasound exerts on the near surface area of the wafer (depth about 100 μm), as a result of such treatment there occurs the stimulated by ultrasound migration of atoms of the alkali metals K, Na from the bulk to the surface. After removal of the surface layer this makes it possible to considerably reduce concentration of the alkali metals in the silicon wafer.

It is to be noted, however, that the methods, which are related to cleaning the bulk of the silicon wafers from the undesirable impurities by means of their transfer to the surface layer with its subsequent removal, cannot be applied at any from the IC fabrication process stages. Due to this cause they remained in low demand during the ICs creation, but find a wide application for study of the control processes of the defect formation in the semiconductor material.

But also the methods of the internal gettering have the considerable limitations and not always can be applied or not always turn out to be effective. This takes place, for instance, in the cases, when:

- are used the mono-crystals with the oxygen contents of less than $5 \cdot 10^{17}$ cm^{-3} or the high-doped silicon wafers of n-type (arsenic or antimony doped), when the precipitation process does not happen;
- are applied the low temperature processes or the fast thermal treatment, when the weakly diffusing atoms of the internode oxygen cannot cover the great distances during the treatment time;
- for creation of the devices is used the entire thickness of the wafer (power devices).

In such cases it is required to apply the external gettering or use combination of the external or internal gettering.

Amongst the used at present methods of the external gettering the most interesting is the well-controlled method of introducing disruptions into the reverse side of the wafer by means of the high energy laser irradiation [43—46]. Meanwhile there occurs the silicon evaporation with formation of the shallow pits, located close to each other, which results in generation of the crystal lattice disruptions and emergence of the mechanical stresses. After irradiation the wafers are subjected to annealing, sufficient for formation of dislocations around the disrupted areas and diffusion to them of the mobile point defects and metal impurities from the wafer's bulk. The important peculiarity of this method is a possibility of formation of a getter at the various stages of the IC creation. Besideso, during formation of a getter on the initial silicon wafers its serviceability may be maintained during the entire process cycle of the ICs fabrication [47, 48].

The depth of disruptions, caused by the laser treatment, during increase of the energy density up to 7 and after 8 joule/cm^2 rises in the linear way, in the interval of 7—8 joule/cm^2 there occurs a sharp jump, which is related with a transition from the silicon melting to its evaporation. During the laser irradiation with the energy blow this range, there happen the surface melting and its subsequent epitaxial re-crystallization, not causing generation of the crystal defects. The laser treatment with the energy higher than the indicated one, results in the silicon evaporation and the subsequent re-crystallization occurs already with formation of the poly-crystal silicon. The emerged during this de-

fects consist of the dislocations of two types [45]. On the periphery of the laser spot there observes a high concentration of the sliding dislocations, which well annihilate during annealing. They are similar to dislocations, emerged during the mechanical methods of disrupting the crystal structure of the wafer. But under the area, subjected to the laser influence, by means of the electron microscopy there were detected the micro-cracks, which get annealed in the process of heat treatment, and the related to them rows of the fixed dislocations, being thermally stable [46]. The energy threshold, when there occurs formation of the micro-cracks on silicon of orientation $|111|$, constitutes approximately 15 joule/cm^2 with the pulse duration of 100 ns. The thermally stable lattice defects at the time of the subsequent thermal treatments act as drains for the point defects.

Concentration defects in silicon is characterized by the life time of the minority charge carriers τ. **Table 2** lists the values τ, obtained after oxidation of ten wafers, one half of which was laser treated. From these data it ensues, that to obtain the effect of gettering the minimum energy density should be not less than 8 joule/cm^2, to which corresponds the disruption depth of h=5 μm. While increasing the disruptions depth efficiency of gettering rises, however, with h=20 μm (E= 33,3 joule/cm^2) the life time τ after heat treatment reduces. This is related to slide of dislocations through the entire thickness of the wafer to its working side. Therefore the optimum for gettering one should consider the depth of disruptions of 5—10 μm, which is attained at E=9—15 joule/cm^2.

Table 2

Efficiency of wafers treatment with the laser irradiation of different power [46]

E, Joule / cm^2	Values τ for a part of a wafer, μs	
	irradiated	without irradiation
9,9	280,3	—
	190,0	100,8
8,2	277,4	103,3
	606,7	3,2
6,5	35,0	8,6
	11,7	40,7
	94,5	211,7
5,3	7,4	9,4
	42.3	70,9
	79,6	9,4

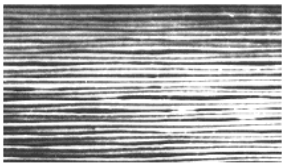
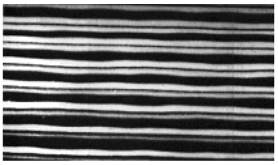
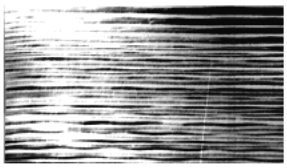
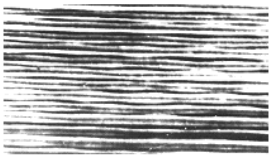
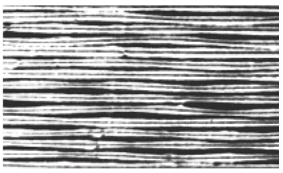
Meanwhile, it is worth to note, that the laser irradiation of nanosecond duration results is the silicon expelling from the irradiation influence area that causes pollution of the working side of the wafer with the silicon dust. Therefore for creation of the gettering area of interest is the laser treatment

in the mode of the heat flow (by a continuous laser irradiation), ensuring silicon melting without its evaporation.

Such an approach was realized for creation of the gettering layer from the non-working side of the silicon wafer during application of the АИГ:Nd^+ laser in the continuous mode of operation. In this case a silicon wafer develops the tensile stresses, whose value reduces with the scan rate increase V and reduction of the power density $E_{м0}$ of laser irradiation (**Table 3**) [49, 50].

Table 3

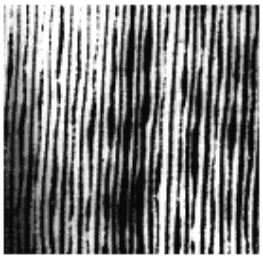
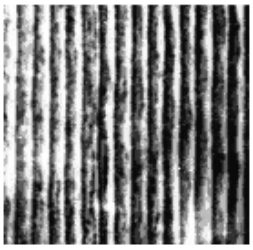
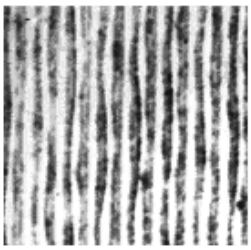
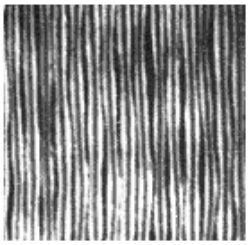
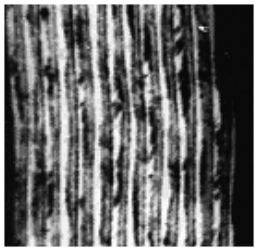
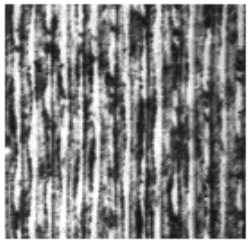
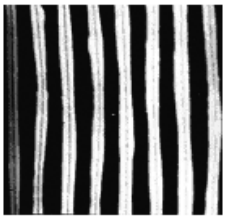
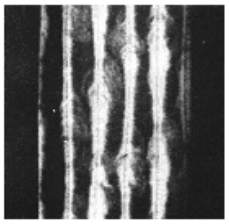
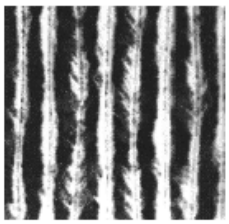
X-Ray topograms of Si-wafers after their laser treatment

Modes of Laser Treatment	Topograms of Si-wafers, treated at various modes	
$E_{м0} = 5 \cdot 10^5$ W/cm^2, V = 60 cm/sec,	H = 200 um 	H = 400 um 
$E_{м0} = 5 \cdot 10^5$ W/cm^2, H = 200 um	V = 40 cm/sec 	V = 60 cm/sec 
V=60 cm/sec, H = 200 um	$E_{м0} = 4{,}5 \cdot 10^5$ W/cm^2 	$E_{м0} = 5 \cdot 10^5$ W/cm^2 

In [51] on the basis of the performed calculation of the temperature fields and experimental results there was determined the required from the point of view of efficiency and overlapping of the stressed areas from the two adjacent scan lines, the mode of laser treatment for formation of the gettering layer: H = 200—240 um, $V \approx 60$ cm/s and $E_{м0} \approx 5{,}5 \cdot 10^5$ W/cm^2. The subsequent prolonged thermal treatment at the temperature of 1100—1200°C in the oxygen medium results in the efficient formation in the area of the laser influence of the dislocation lattice and oxygen precipitates, being the centers of gettering (**Table 4**).

Table 4

X-ray topograms of Si-wafers, undergone the thermal treatment at the different temperatures after the laser irradiation with the various rate and a pitch of scan with the power density of $5{,}5 \cdot 10^5$ W/cm^2

Modes of laser treatment	Temperature of thermal treatment		
	900°C	1150°C	1220°C
V=40 mm/sec, *H* = 200 um			
V=60 cm/sec, *H* = 200 um			
V=60 cm/sec, *H* = 400 um			

Creation of such gettering layer prior to the thermal oxidation at the temperature, exceeding the temperature of the subsequent extended high temperature processes, ensures a 220—440 times reduction of the packing defects and dislocations density (**Fig. 1**), to have a 2,9 times reduction of the fill-up ratio with the slide lines in the epitaxial films, to have a 12 times rise of the life time of the minority charge carriers and the recombination life time in silicon (**Fig. 2**), as well as to reduce 1,8 times the density of the surface states on the separation boundary «silicon — thermal silicon dioxide» [52, 53]. The thermally grown on such wafers the silicon dioxide films possess the improved structure, a higher charge stability and the high quality separation boundary.

Application of gettering with application of the continuous laser irradiation in the technology of creation of the bipolar ICs makes it possible at the expense of the propagation reduction of the slide lines, reduction of the dislocations density in the epitaxial film and exclusion of the conducting shunts emergence in the area of the active and passive elements to eradicate degradation of the breakdown voltages «collector — emitter» and the consumption currents. This ensures a two times increase in the yield of the good devices on the wafer and a 11,6% rise in the yield of the good devices after their assembly and measurement of the electric parameters [54]. In creation of the MOS IC such a method of gettering makes it possible at the expense of the threshold voltage reduction, determined by the charge

reduction on the separation boundary «Si — SiO_2», to exclude its degradation and, consequently, to increase (1,5 times) yield of the good devices.

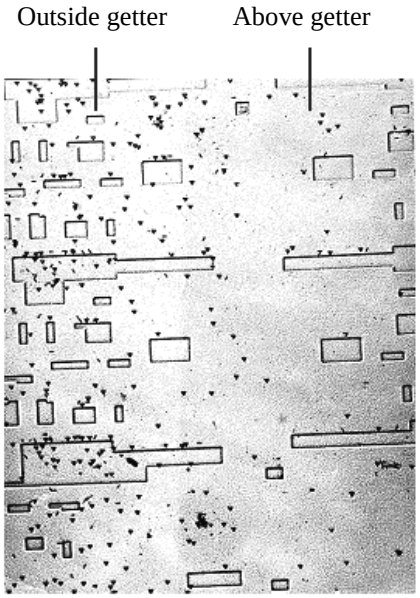
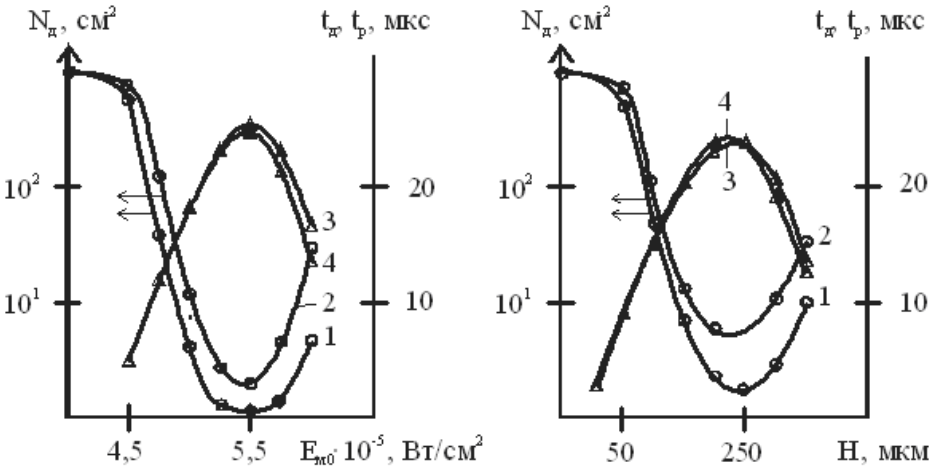


Fig. 1. View of the decorated surface of the epitaxial silicon film after gettering

a) b)



c)

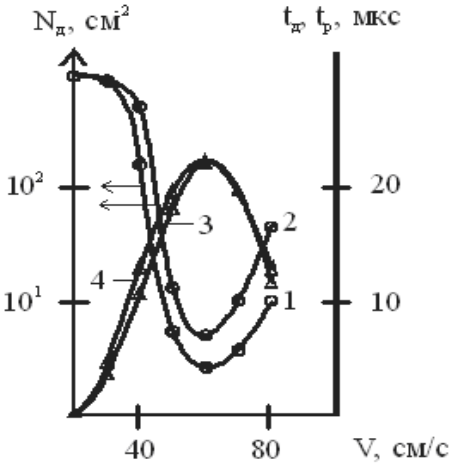
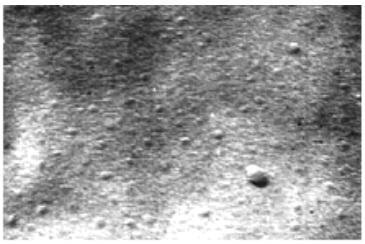
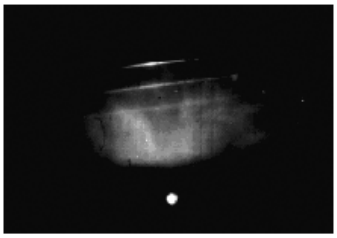
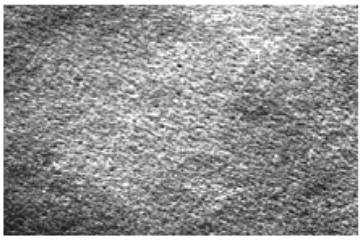
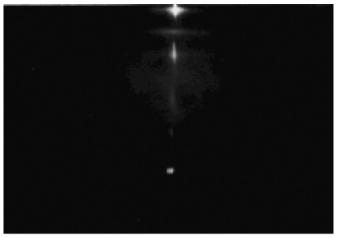
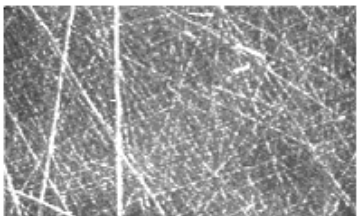
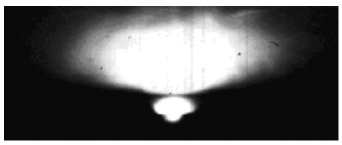


Fig. 2. Dependencies of the electro-physical parameters of Si-wafers after gettering on the power density of the continuous laser irradiation (*a*), pitch (*b*) and scan rate (*c*):
1 — density of packing defects $N_д$;
2 — density of dislocations;
3 — life time of the minority charge carriers τ;
4 — recombination life time $\tau_р$

In order to clean the working side of the silicon wafers from the admixture impurities of interest is the treatment mode by the laser irradiation of nanosecond duration (20—30 nsec), when melting occurs of the surface layer and its subsequent re-crystallization without introduction of any disruptions into the crystal lattice of this layer [55—57]. Analysis of such wafers' surface after the thermal oxidation shows, that after removal of the oxide film and etching the surface in the selective etchant the structural defects are not in evidence, peculiar for the thermal oxidation of the untreated wafers. This is related to the fact, that during melting of the thin surface layer there occurs its purification from the ions of metals and carbon owing to their diffusion via the liquid flux to the surface and the subsequent evaporation, as well as eradication of the upset by the chemical-mechanical polishing surface layer (**Table 5**) [56, 57]. This is confirmed by the results of the comparative analysis of the structure of dielectric films, cformed by means of the thermal oxidation in the dehydrated oxygen medium of the silicon wafers of the *n*-type conductivity, before and after the laser treatment of the surface.

Table 5

Surface structure of the silicon wafers, subjected to the chemical-mechanical and mechanical polishing before and after treatment with nanosecond pulses

Performed treatments		Micro-reliefs of surfaces	Images of diffraction
Chemical-mechanical polishing	Before laser treatment		
	After laser treatment		
Mechanical polishing	Before laser treatment		
	After laser treatment		

Surface structure of the silicon wafers after treatment with the laser pulses is more uniform, as the wafer surface has no disrupted layer and ion admixtures, which result in the increased vapor forma-

tion and disruption of continuity of the formed layer, as well as create the crystal phases. About purification of the surface layer from the ion impurities after the laser treatment indicates reduction over two times of the fixed charge on the separation boundary «silicon — thermal silicon dioxide», as well as the spectra of the fast surface states, whose density in the middle of the denied zone in the section with the laser treatment is two times less, than in the untreated one [53].

However, application of such cleaning is limited, as it cannot be used at the different stages of IC creation — it can be conducted only on the initial wafers, prior to the moment, when on the surface there will be formed any functional layers.

Thus, application of the laser irradiation of nanosecond duration makes it possible to conduct purification of the working surface of the initial wafer from the ion impurities. For the efficient purification of the surface layer from the working side of the wafer from the uncontrolled impurities by means of gettering the most prospective is application of the continuous laser treatment for the controlled formation of the of the gettering centers from the non-working side of the wafer. The important advantage of such method is the possibility of its application at the various stages of ICs creation, and absence of any requirements on the special preparation of wafers points out its application justification in the VLSI technology.

Majority of methods of gettering was found by the empirical way and used in the ICs fabrication technology without determining a mechanism of their passing. For the considered above methods of gettering we will determine the possible mechanisms of interaction of the admixture defects with the point ones, being for them drains in the process of gettering.

As the admixture defects introduce the elastic tensions into the surrounding them matrix, their interaction with the external tensions brings movement and a build-up of the admixture defects in the areas of point defects.

The external tensions may have the macro- and micro- and non-homogeneous nature. The first, so called macro- non-homogeneous external forces, act on the entire ingot or a wafer. N case of the silicon wafer they emerge during application on its reverse side of the films Si_3N_4 and Al_2O_3. Thus, for instance, in the film of Si_3N_4 the internal tensions reach 10^9 N/m^2 and are balanced with the elastic tensions in the silicon wafer, which, in their turn, cause the directed movement of the admixture defects.

Tensions of the micro- non-homogeneous nature in silicon are caused by the linear, flat and bulk defects. Interaction of these defects with the admixture ones may be subdivided into the four kinds: those, caused by the difference in the sizes of the admixture defects and atoms of the matrix (array); caused by the difference in the elasticity models; chemical ones; electric ones. They all result in the non-uniform distribution and concentration of the admixture defects near dislocations, boundaries of grains, etc. Extrusion of the excessive admixture defects starts at the edge dislocations, and with their great saturation – at all dislocations, and this means, that with the small saturations the nuclei at the edge dislocations determine the entire kinetics of extrusion.

The high density of dislocations is attained by means of the high temperature phosphorus diffusion [58], ion implantation [59, 60], mechanical treatment [61—63], laser irradiation [47, 48]. Meanwhile, the energy and doze of ion implantation, as well as density of the laser irradiation energy should be sufficient for their formation.

Investigation of the copper gettering by means of the ion doped layer [61] showed, that dislocations with the Burgers vector $b=a/2<110>$ possess a great capacity for the copper gettering, than the partial Frank dislocations with $b=a/3<111>$, which is accounted for by their great energy of the elastic field. In [61] it was established, that with the doze of ion implantations up to $6\cdot10^{13}$ cm^{-2} there emerge the packing defects, surrounded by the partial Frank dislocation, and the packing defects with the dislocation loops transform into the full dislocations with $b=a/2<110>$, which with a higher implantation dose for the dislocation grid. A considerable efficiency increase of gettering occurs with the dose of $3\cdot10^{14}$ cm^{-2}, when there is a great density of dislocations. Efficiency of such gettering in [61] was assessed by the relaxation leakage current of the disbalanced MOS-capacity. Increase of the leakage currents with the doses of $3\cdot10^{15}$ and $6\cdot10^{15}$ cm^{-2} as compared with a dose of $3\cdot10^{14}$ cm^{-2} is explained by precipitation of the implanted impurity at dislocations. I. e. the required component of the microstructure of the gettering ion-doped layer is availability of dislocations with $b=a/2<110>$. Density of these dislocations with the high free energy, ensuring the efficient gettering, is assessed as $2\cdot10^{8}$ cm^{-2}.

If the impurity defects create the charged centers, i. e. are the donors or acceptors, then on their distribution exerts influence concentration of electrons or holes. Consequently, creating the non-uniform distribution on the wafer of the donor or acceptor impurity in the sufficiently great concentrations, one can expect the non-uniform distribution on the wafer and other charged admixture defects, for instance, the fast diffusing metals. Thus, it is possible to getter the undesirable admixture defects from the ICs active areas into the specially doped non-active areas. Phosphorus gettering of gold takes place as per the given mechanism. Gold takes mainly the replacing position, and vacancies interact with the phosphorus atoms with formation of the *E*-centers [64]. Gold dilution in silicon of its inherent conductivity occurs with interaction of the atoms of gold with the free vacancies, which was experimentally confirmed by means of the leakage current control of diodes after the subsequent operations of heat treatment of the wafers [58]. The considered mechanism of gettering is applicable not only for gold, but for other heavy metals as well [65]. The low temperature ($800^{o}C$) gettering with phosphorus is effective in that case, if silicon does not contain precipitates of heavy metals. If such precipitates are available. Then for their dilution annealing is required at the high temperature ($1000^{o}C$). Thus, the diffusion area getter the fast diffusing impurities both by means of the ion interaction and owing to the mechanical tensions near dislocations.

Another mechanism of gettering is absorption of the admixture defects by the liquid or liquid-like phase. It is known, that the balanced distribution ratio k_0 in silicon for majority of impurities is less than one [66]. For instance, for copper the distribution ratio in silicon constitutes $4\cdot10^{-4}$, for gold

— 10^{-15}, for iron — 10^{-15}. If in any part of the wafer to create a liquid phase, then its remaining part can be purified from impurities with k_0<1. Insertion into silicon of a great number of disruptions of the crystal lattice imitate the liquid-like phase [67], and during the thermal treatment this phase getter the impurities with $k_0 < 1$ from the remaining, undisturbed part of silicon. Such upset liquid-like phase is created on the back side of the wafer during insertion into it the disruptions of the crystal lattice by the mechanical method (for instance, grinding), ion implantation of argon, high temperature phosphorus diffusion, laser irradiation, etc.

Gettering may also take place owing to extraction of the admixture defects into vacuum or gaseous phase. During the high-temperature annealing of the Si-wafers in the neutral atmosphere or in vacuum there occurs evaporation of the silicon atoms and admixture from the surface. Concentration increase of vacancies (concentration reduction of the inter-node atoms) on the surface relative to balanced in bulk results in diffusion of the inter-node atoms to the surface, reduction of the packing defects and formation in the surface layer of the defectless area. During evaporation the system «silicon — impurity» loses the volatile component, releasing silicon from the easily evaporated admixture. Addition of HCl and trichloroethylene into vapor gaseous mixture during oxidation results in the similar effect. At the high temperature the silicon atoms are pulled by the molecules of HCl, reaching the surface of partition «Si — SiO_2», into the oxide layer and get oxidized there [68]. Meanwhile, concentration of vacancies on the surface increase as compared with the balanced one. Number of the extracted silicon atoms from the silicon surface into oxide and, appropriately, the surface concentration of vacancies increase with the concentration increase of HCl and the oxidation temperature [69].

The gettering mechanism may be also adsorption of the impurity defects on the developed surface. In this case the solid body surface adsorbs them, reducing its free energy. By increasing the surface area in the non-active areas of the wafer it is possible to extract the admixture defects there. By this mechanism occurs gettering of impurities by means of the porous silicon, formed on the back side of the wafer [24].

An important mechanism of gettering, that is always present during the laser or fast thermal treatment, is extraction of the impurity, distributed in the near surface area of the semiconductor wafer, on its surface with a great temperature gradient, perpendicular to the wafer. On the basis of consideration of the 1D flow of the impurity atoms, related to the temperature gradient, in [41] it is indicated, that with the preset grad$T$ the heat transfer value determines the value and direction of the impurity flow in the non-uniform temperature field. This signifies, that on all impurity atoms the force is applied, determined by the temperature gradient and directed to the wafer surface. As the surface is reflective, nearby it occurs accumulation of the impurity, which under the definite conditions may evaporate from the surface, thus purifying the surface from the admixture defects.

The mechanism, promoting transfer of the admixture defects to the surface and its subsequent evaporation, is the liquid phase re-crystallization of the silicon working surface under influence of the

laser irradiation of the nanosecond duration. During such treatment within the first 10—20 ns of the laser pulse there occurs the silicon melting, and the temperature in the flux reaches the values, far exceeding the melting temperature of the irradiated material. In such state the surface layer keeps on remaining during approximately 250 ns, which initially exceeds duration of the laser pulse. The melting edge quickly spreads into the crystal to the depth of the order of 1 μm during the time stretch, just a little exceeding the pulse duration. Then the flux edge moves in the reverse direction to the surface, recrystallizing as it progresses in motion. Meanwhile the molten layer grasps the admixture defects, determined by such admixtures as, for instance, Fe, Ni, Cr, Cu, Na, K, C, as well as the point defects. As a result of their diffusion via the liquid flux and the re-crystallization edge force-out they emerge on the wafer surface and evaporate, thus forming the thin (about 1 μm) surface layer, free from the admixture defects.

An important role during gettering is played by such mechanism, as a grasp of the admixture defects by the oxygen precipitates, which may be formed both with application of the special thermal treatments [39, 40] and with application of the laser irradiation [70].

The formation mechanism of the oxygen precipitates requires for its realization availability in the silicon wafers of the oxygen concentration above the critical one and performance of their thermal treatment in three stages. At the time of the first stage at the high temperaturee (T_1=1100—1200°C) depletion dominates the near surface zone with oxygen, whose process is described by the equation of the impurity diffusion from the limited source with the binding boundaries. As a result, at the expense of the oxygen evaporation, the oxygen depleted near surface area is formed. At the time of the second annealing at the low temperature (T_2=600—800°C) there occurs the homogeneous nucleation (emergence of the precipitation centers) of oxygen. At the time of the third stage at the temperature of T_3>900 °C there simultaneously occurs evaporation of oxygen from the wafer surface and growth of the oxide precipitates. The clean zone is formed because of the fact, that those nuclei, which have grown at the temperature T_2 and had the radius less than critical at the temperature T_3, get diluted at the time of the third annealing, and the nuclei with the radius over critical, vice versa, grow in the oxygen precipitates, which perform the role of gettering centers. Meanwhile, the distribution profile of the oxygen precipitates by thickness of the silicon wafer has such a nature, that the near surface zone of the silicon wafer becomes clean from them, and, consequently, pure from the admixture defects, which get grasped by the oxygen precipitates, lying below the clean zone [71, 72]. In the described formation model of the internal getter, the nature of oxygen precipitation almost completely is determined by the initial concentration of oxygen, incubation time of the precipitation centers origination, by sequence and modes of the thermal treatments.

In application of the continuous laser irradiation the process of gettering passes at the expense of action of two factors — curve of the silicon wafers and occurring meanwhile stretching tensions, which promote formation of precipitates in the gettering layer, ensuring the high efficiency of the puri-

fication process of the working side of the wafer from the impurity pollutions and point defects. The main cause of unavailability of the diffusion flow of admixtures from the gettering layer into the bulk of the wafer with the subsequent high temperature treatments is their capture by the oxygen precipitates, whose emergence promotes formation of the liquid phase of silicon during the laser treatment and the subsequent continuous high temperature treatment in the oxygen medium [70].

On the basis of the considered processes, passing in the silicon wafers during their purification from the admixture defects by the various methods, it is possible to highlight the following mechanisms of interaction of the point defects and polluting admixtures, owing to which gettering occurs:

- interaction of the admixture defects with the field of elastic tensions;
- electric interaction of the admixture defects amongst themselves;
- absorption of the admixture defects by the liquid or liquid-like phase;
- extrusion of the admixture defects into vacuum or gaseous phase;
- adsorption of the admixture defects on the developed surface of the solid body;
- diffusion of the admixture defects to the surface under influence of the temperature gradient through the wafer thickness;
- transfer of the admixture defects by the edge of the liquid phase re-crystallization to the irradiated surface;
- absorption of the admixture defects by the oxygen precipitates.

To the individual methods of gettering there may correspond both a single or several methods, meanwhile, the greater their number for the given method, the more efficient the process will pass of the silicon purification from the point defects and polluting admixtures.

Thus, one may conclude, that during selection of the gettering method of the silicon wafers it is necessary to consider the following:

- availability of the maximum possible number of the interaction mechanisms of the point defects and polluting admixtures, owing to which the gettering process goes on;
- possibility of the method application both at the various creation stages and during duration of the entire process cycle of ICs fabrication;
- flexibility and simplicity of the gettering centers formation in silicon;
- compatibility of the gettering process with the technological process of ICs creation.

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